

FIG. 1

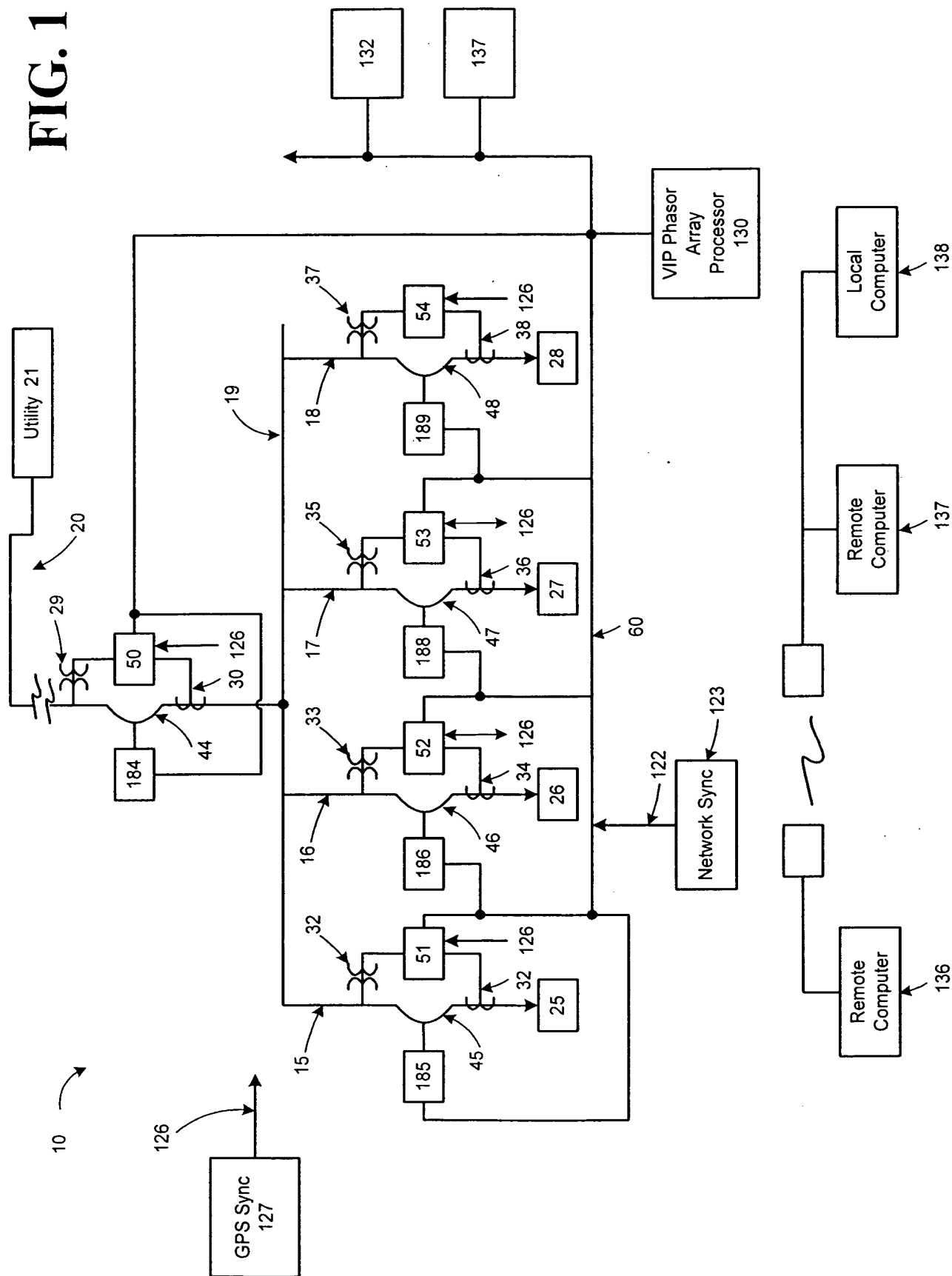
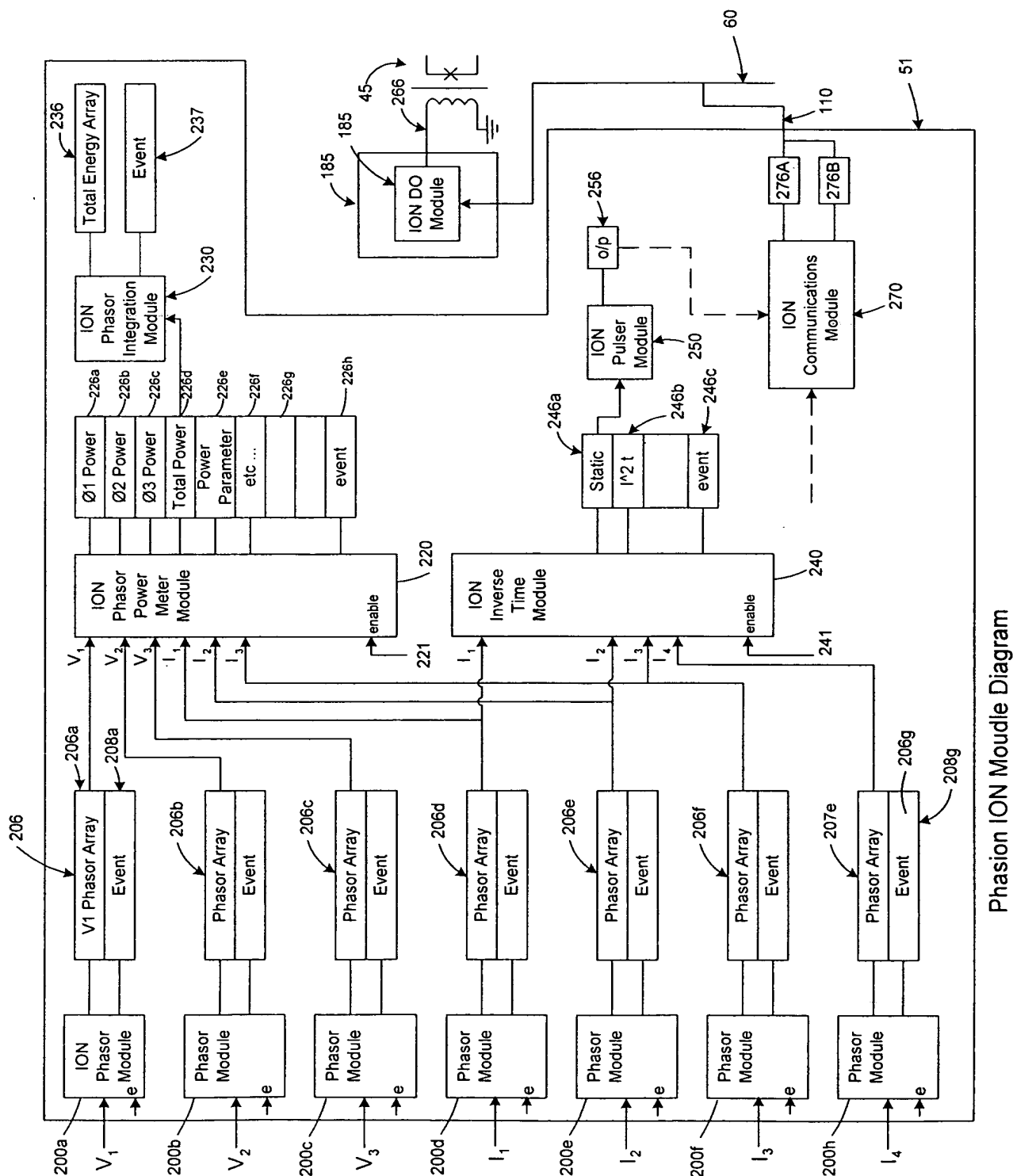


FIG. 3



Phasor ION Module Diagram

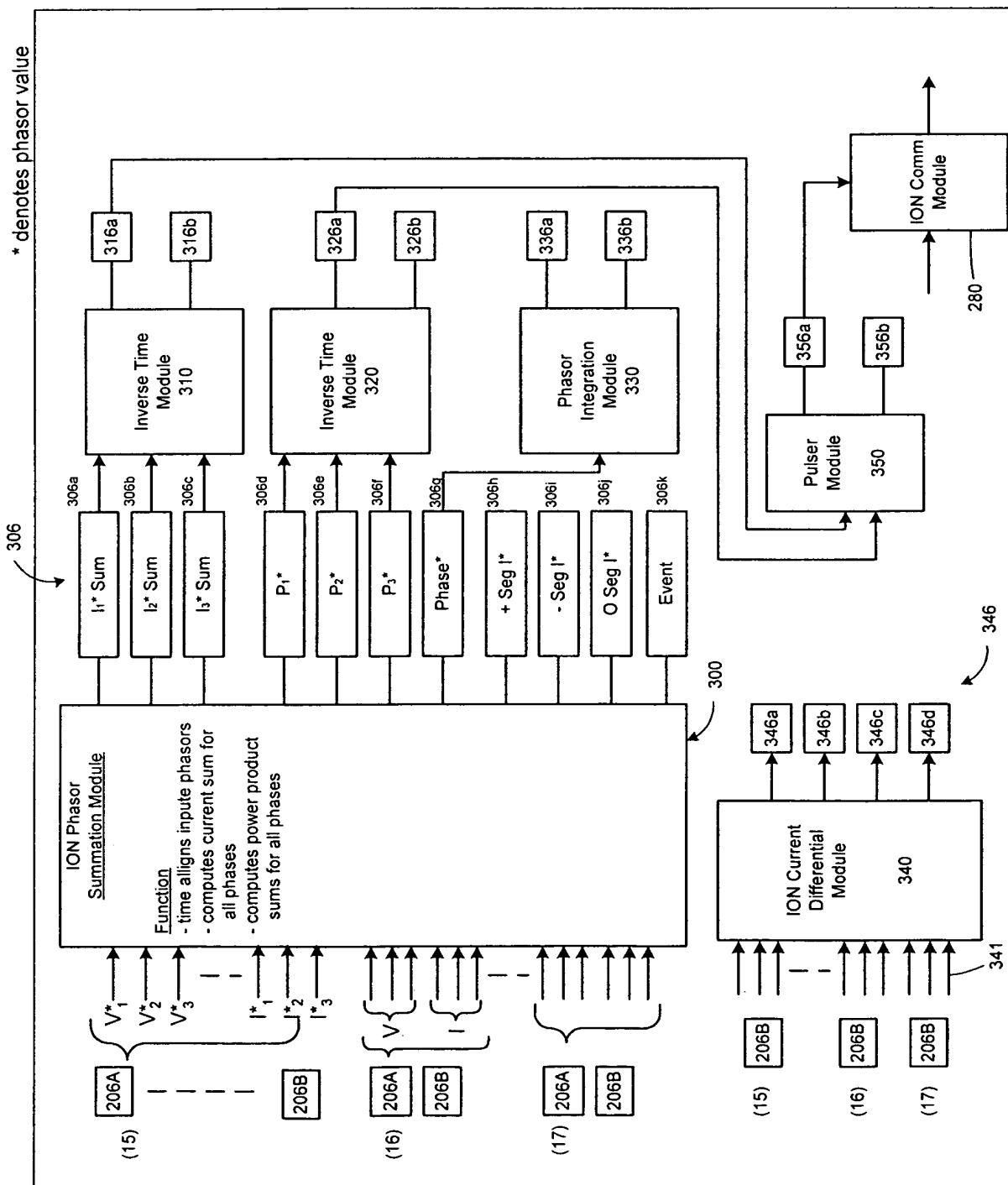


FIG. 4

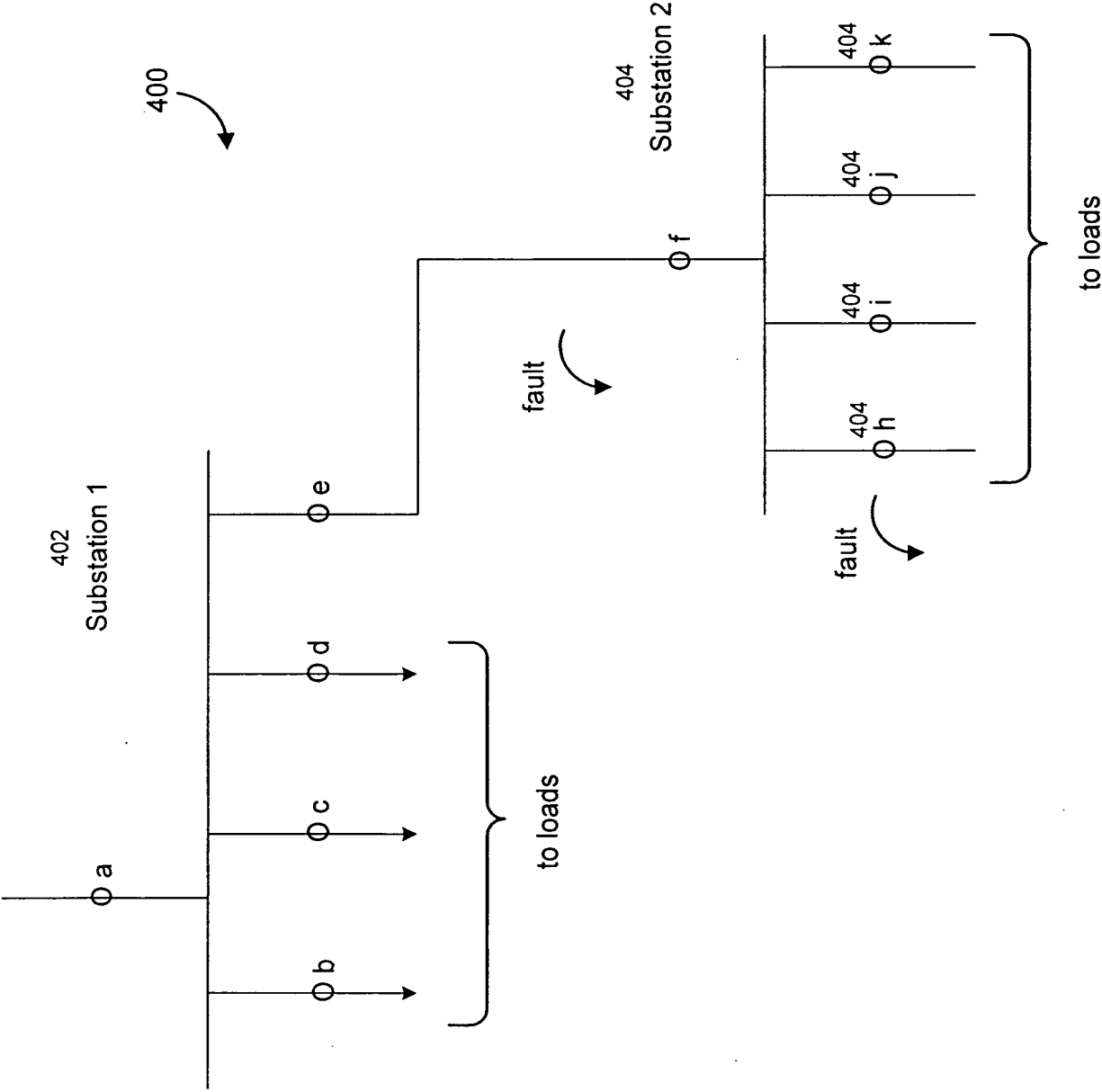


FIG. 5

FIG. 6

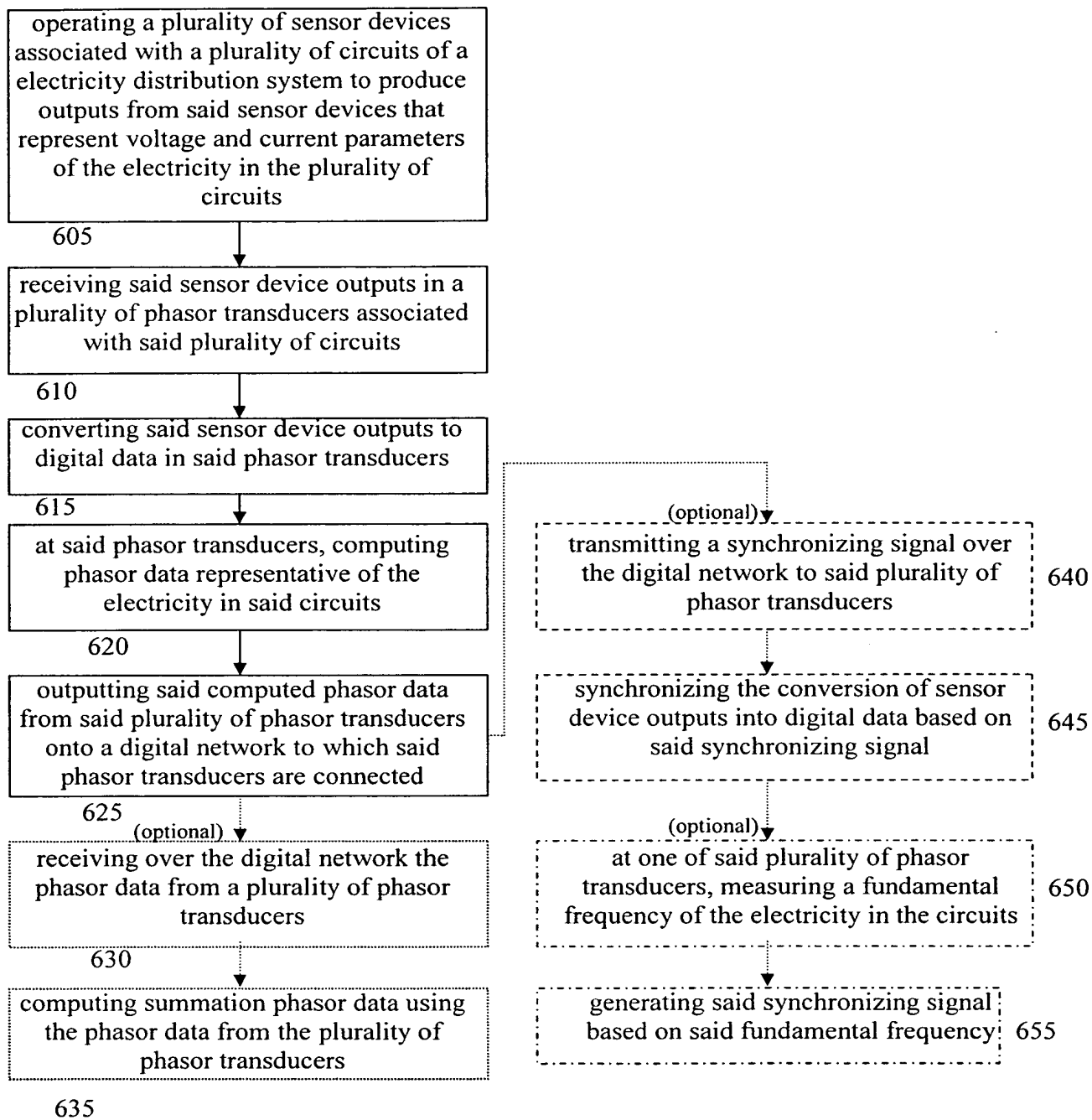


FIG. 7

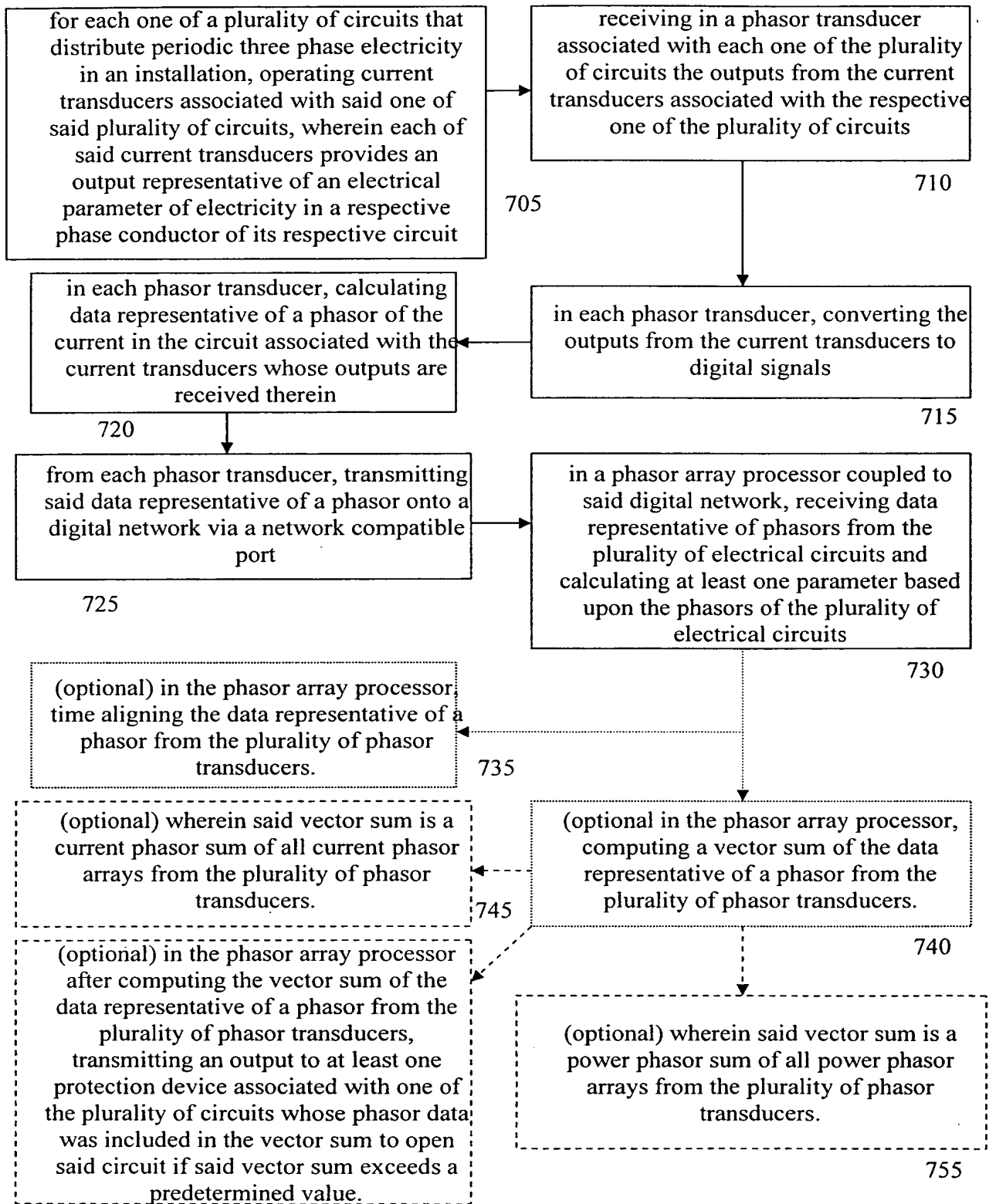


FIG. 8

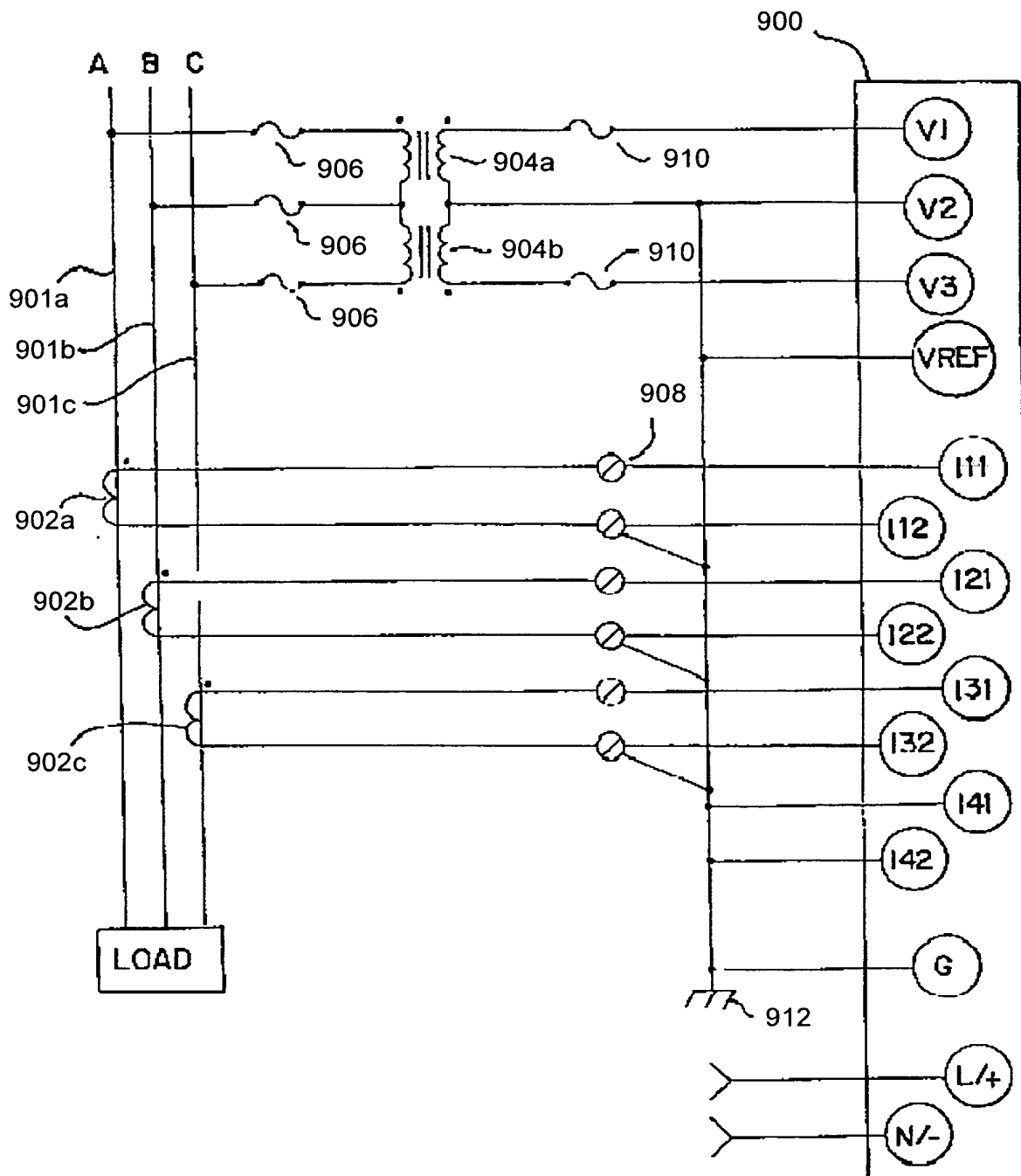




FIG. 9

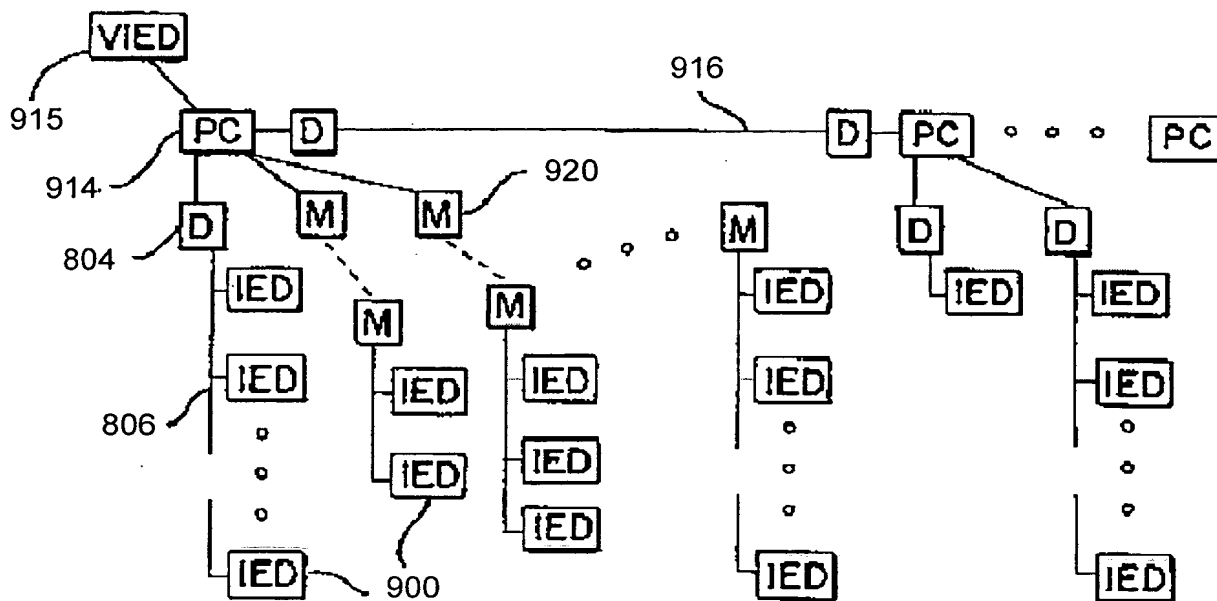


FIG. 11

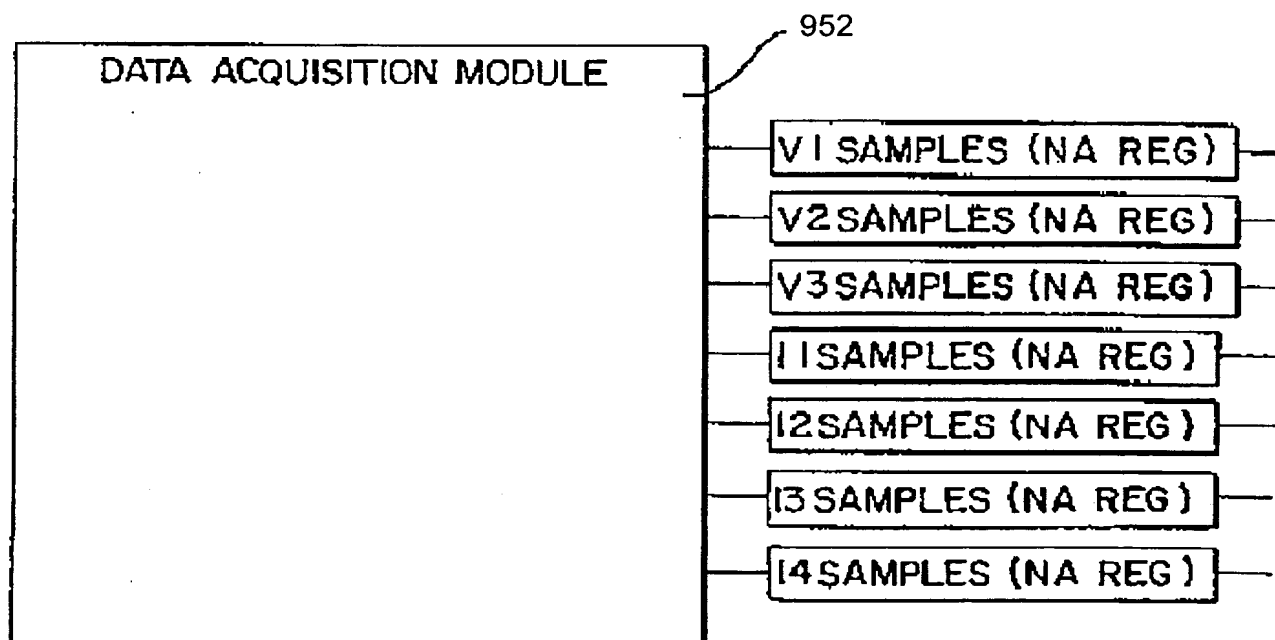
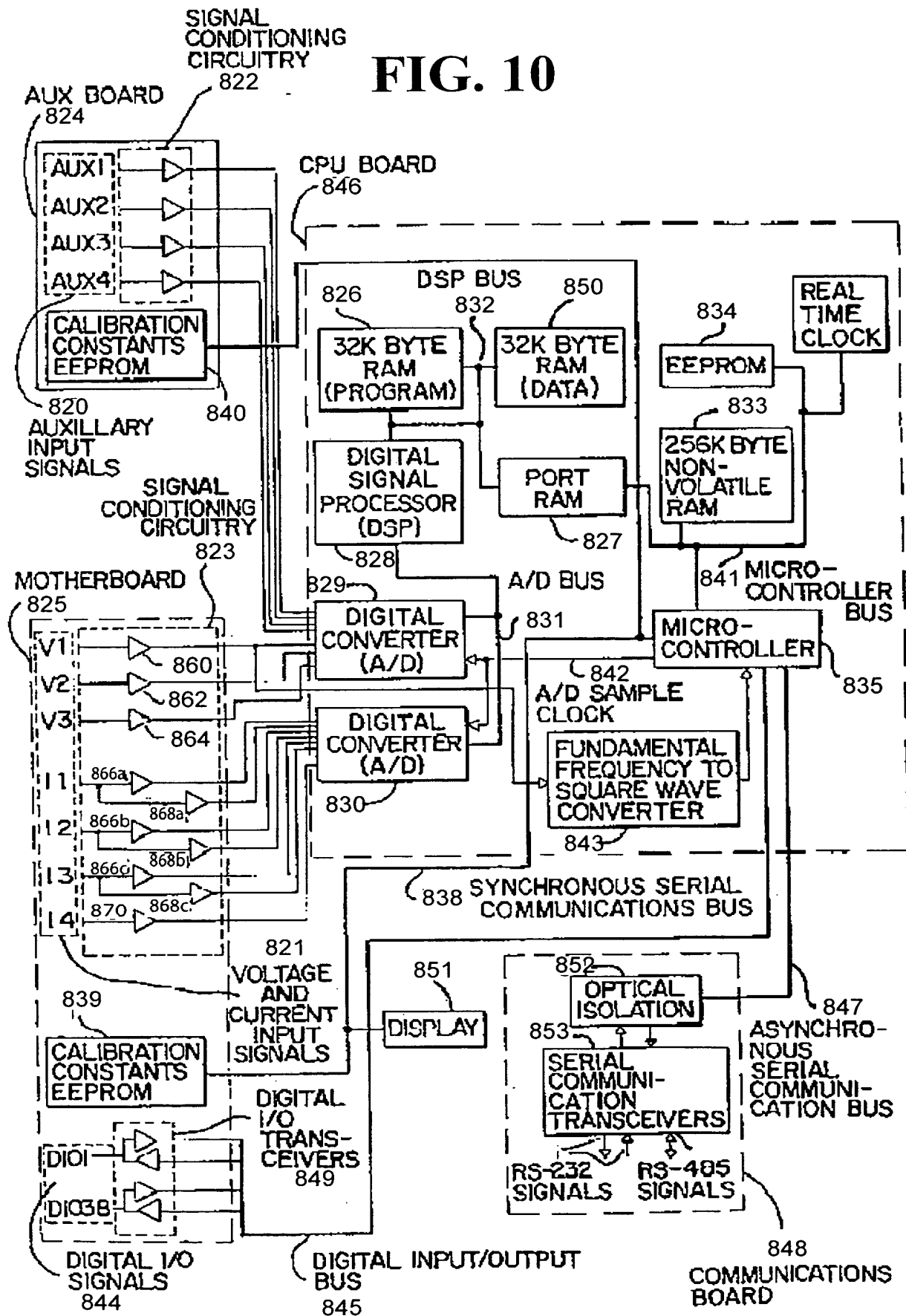


FIG. 10



DATA ACQUISITION
MODULE
OPERATION (CLIENT
PORTION)

FIG. 11A

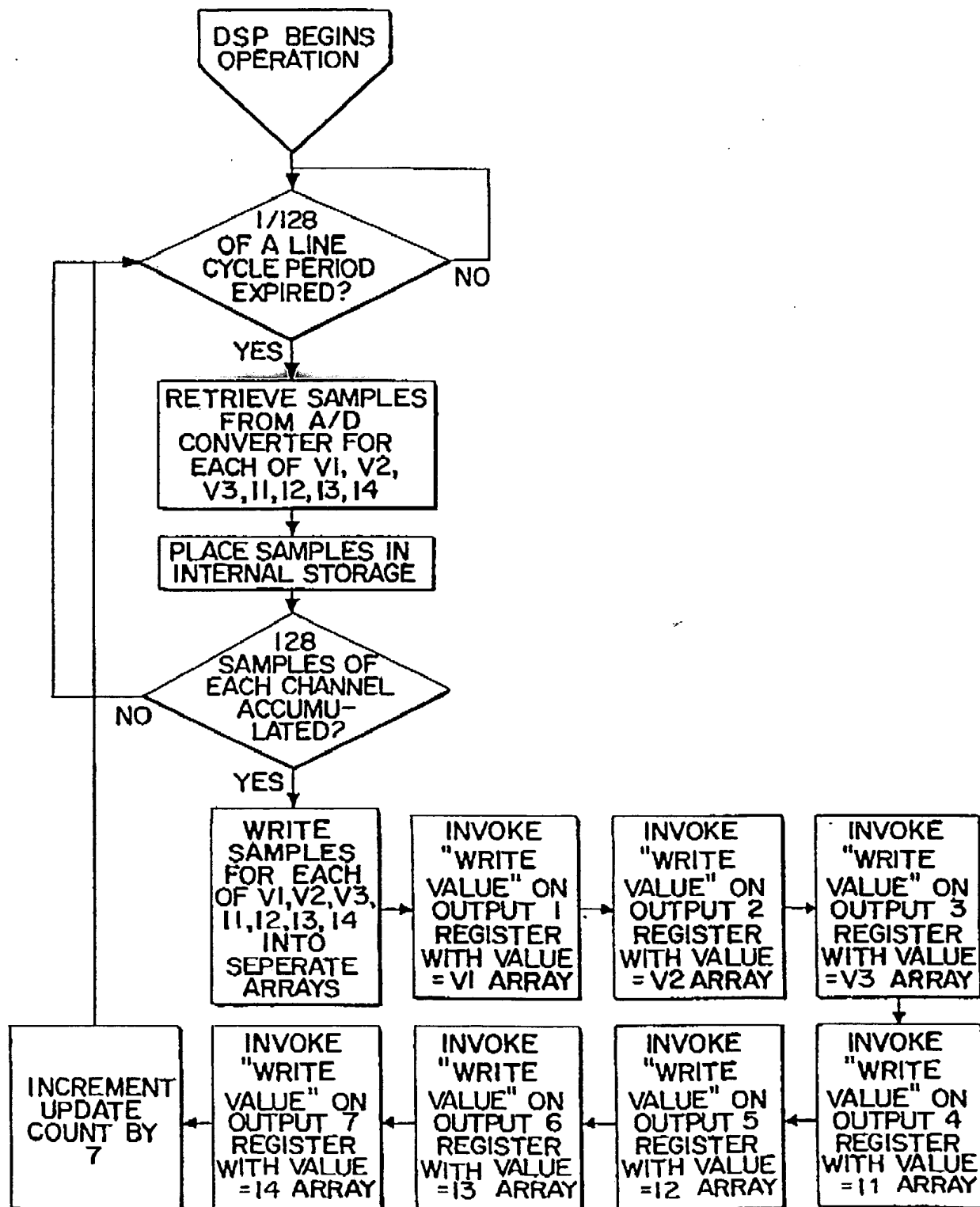
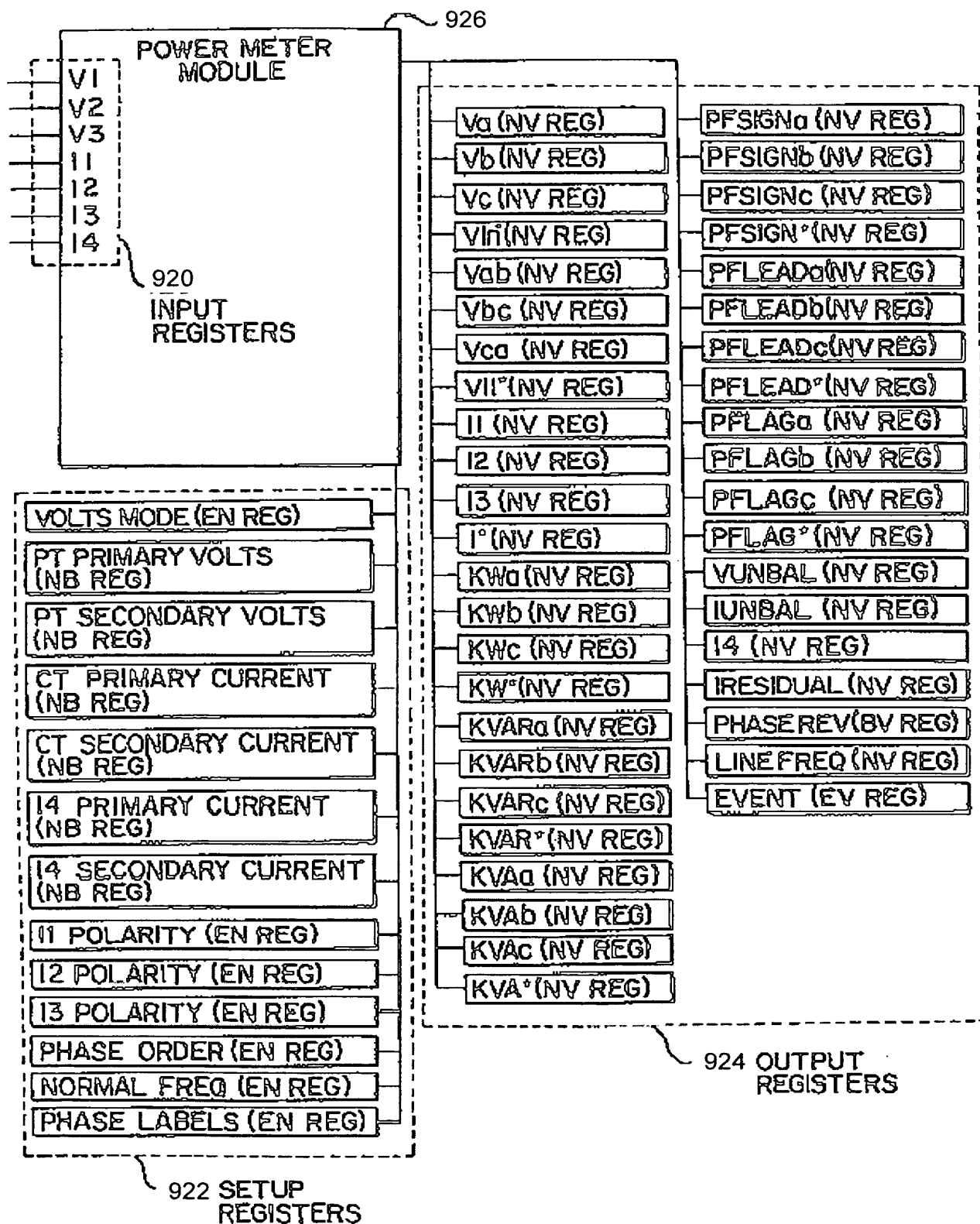
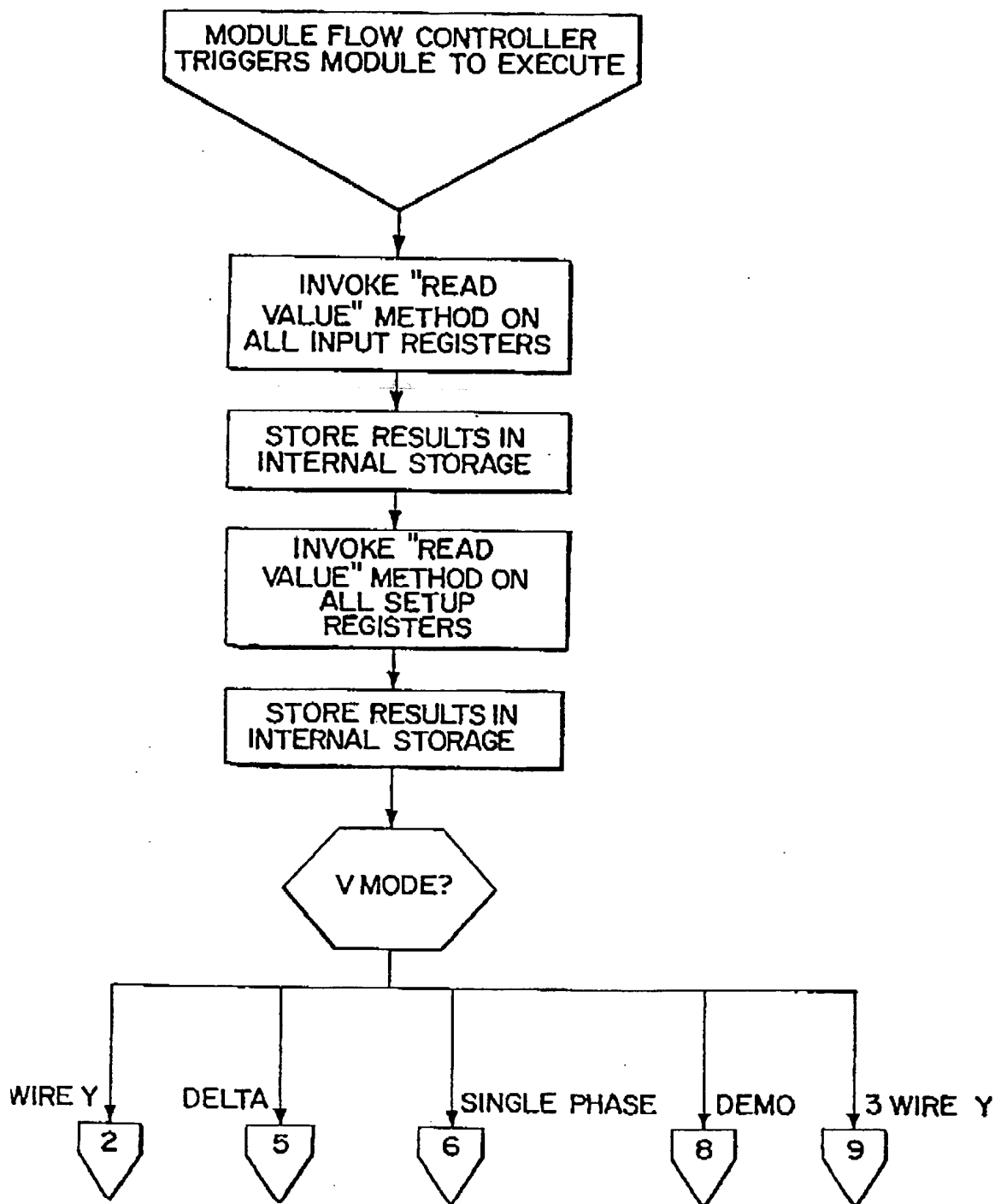


FIG. 12



POWER METER
MODULE
OPERATION
(CLIENT PORTION)

FIG. 12A



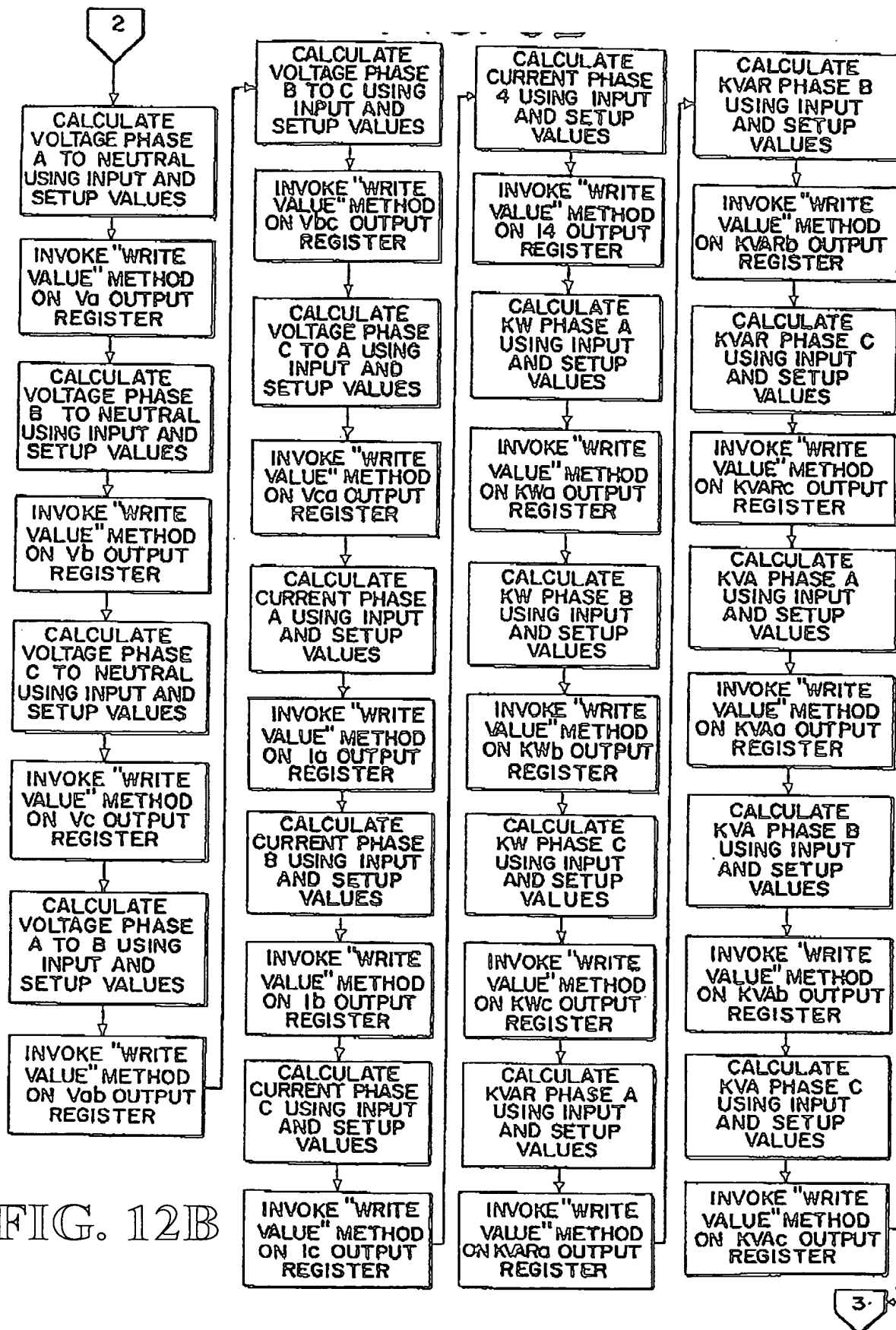


FIG. 12C

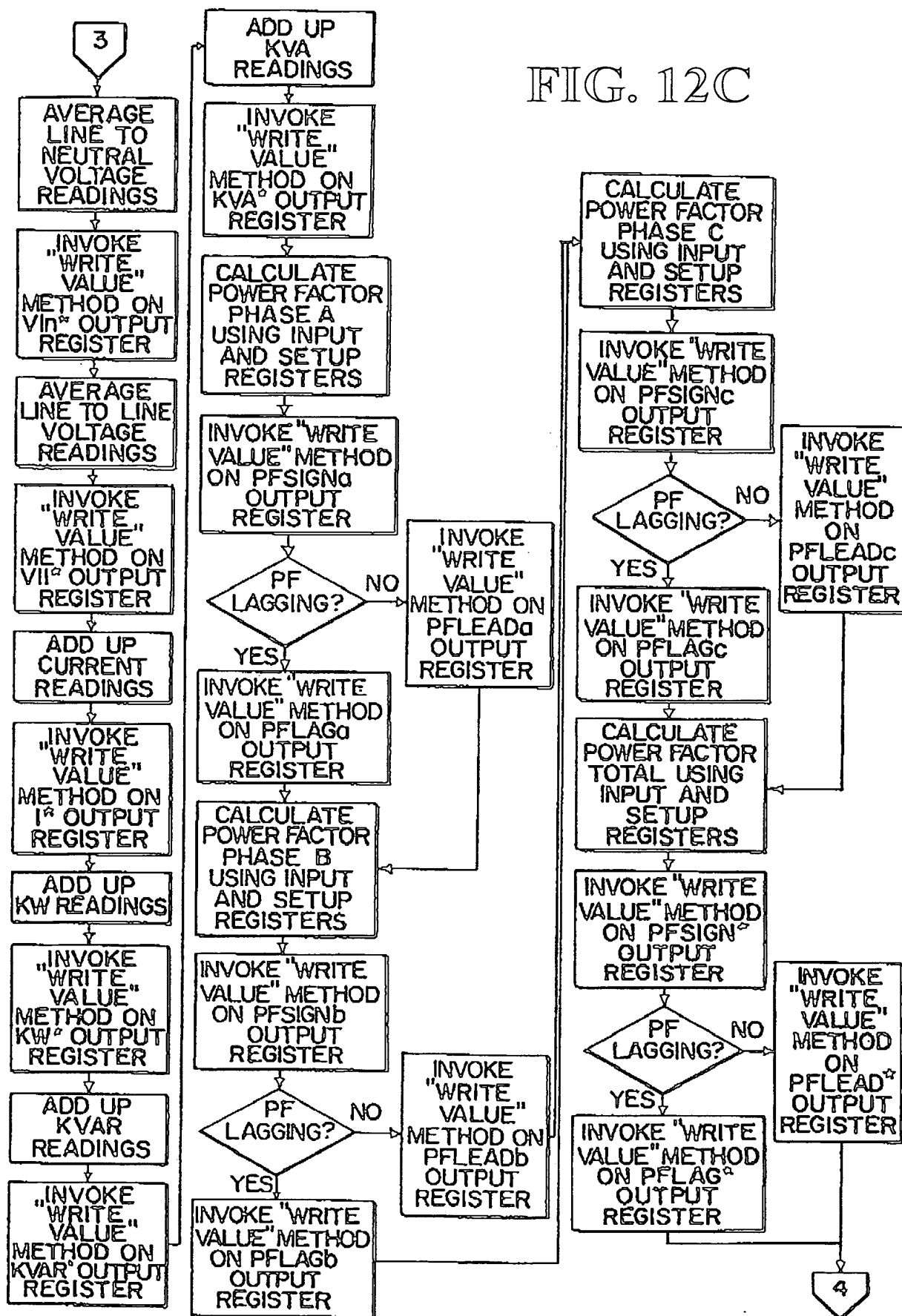


FIG. 12D

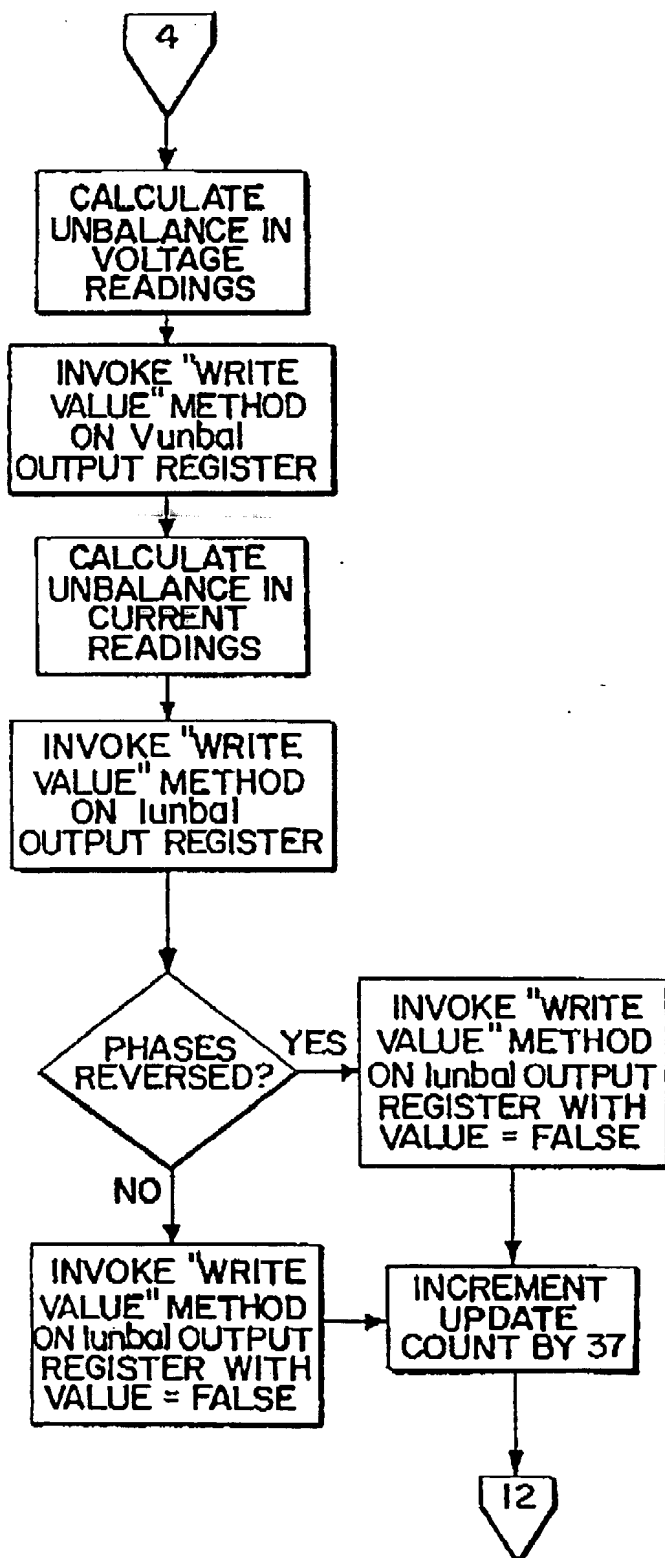


FIG. 12H

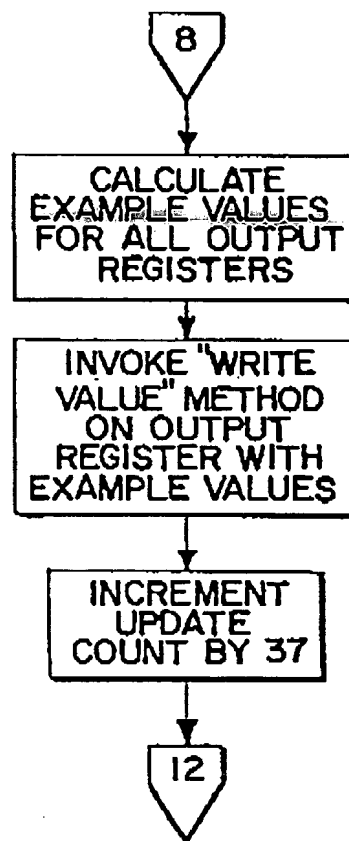


FIG. 12E

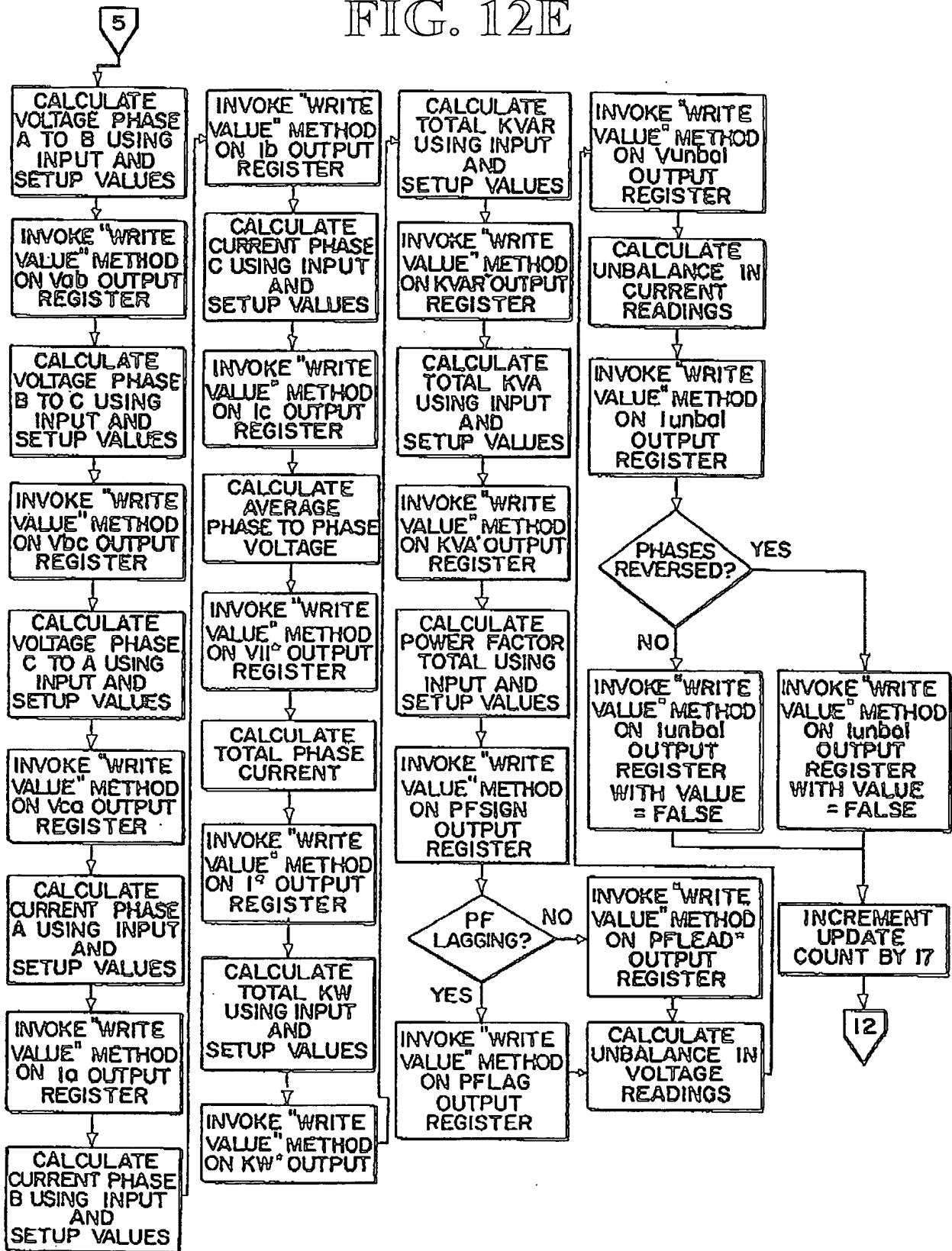


FIG. 12F

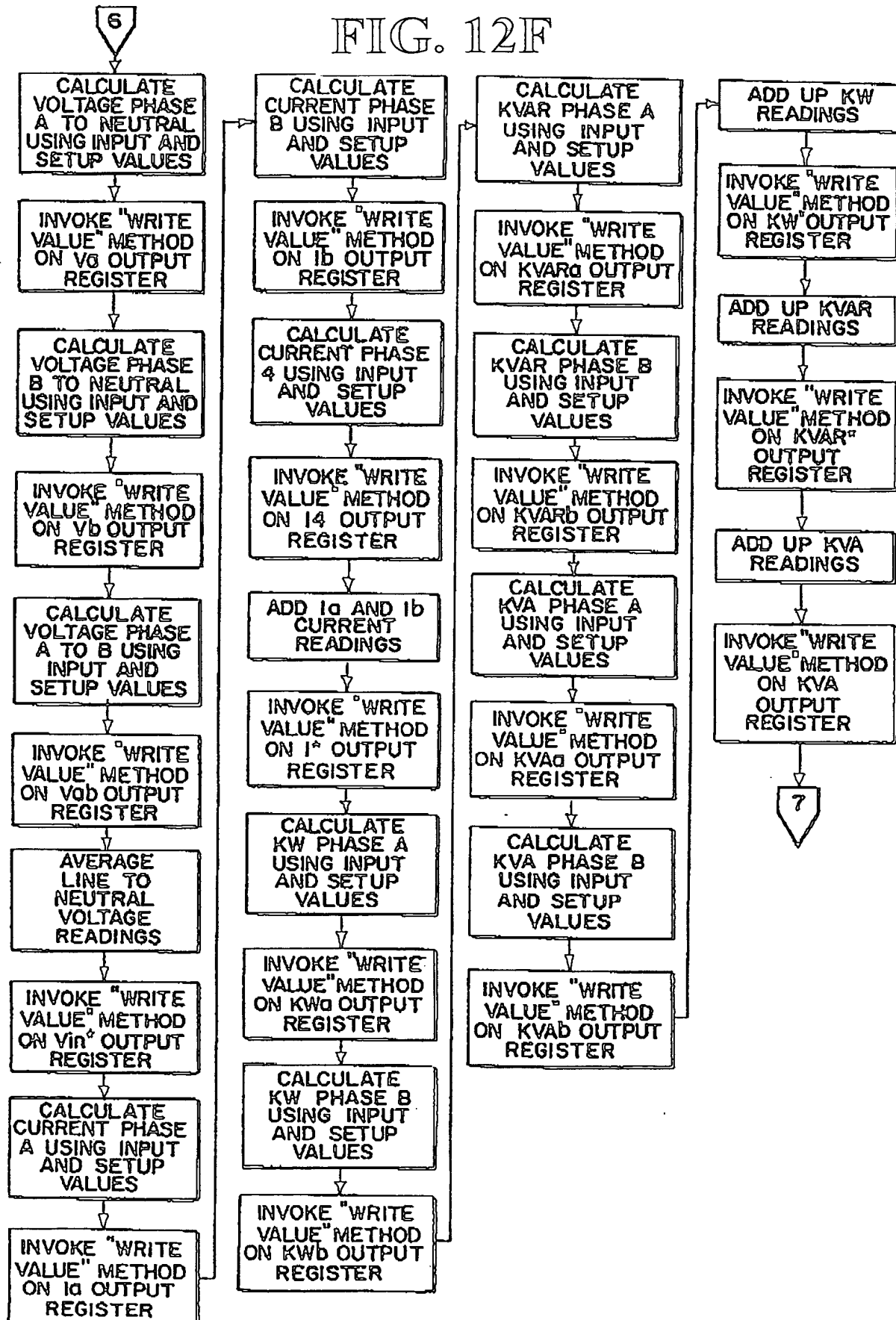
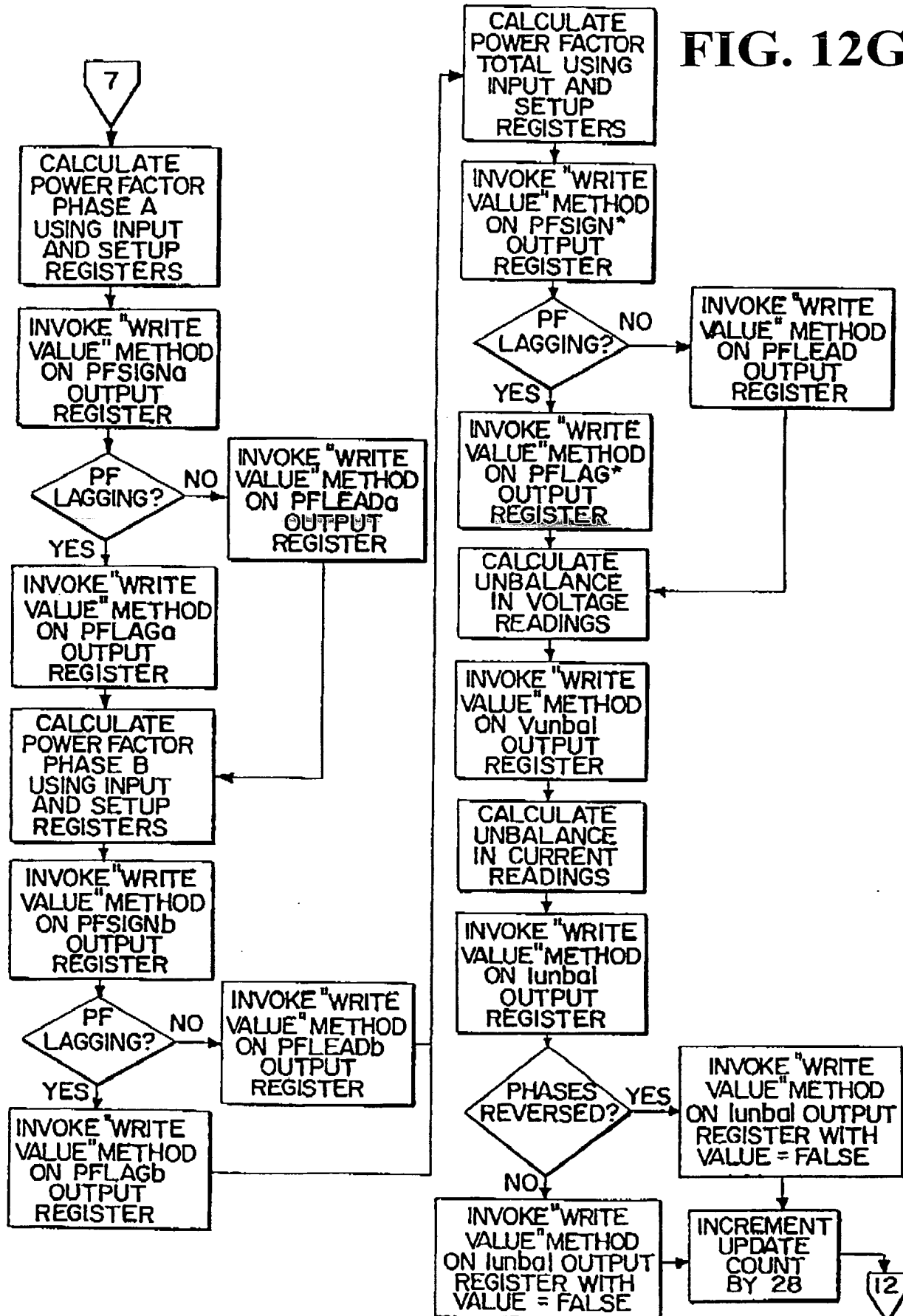


FIG. 12G



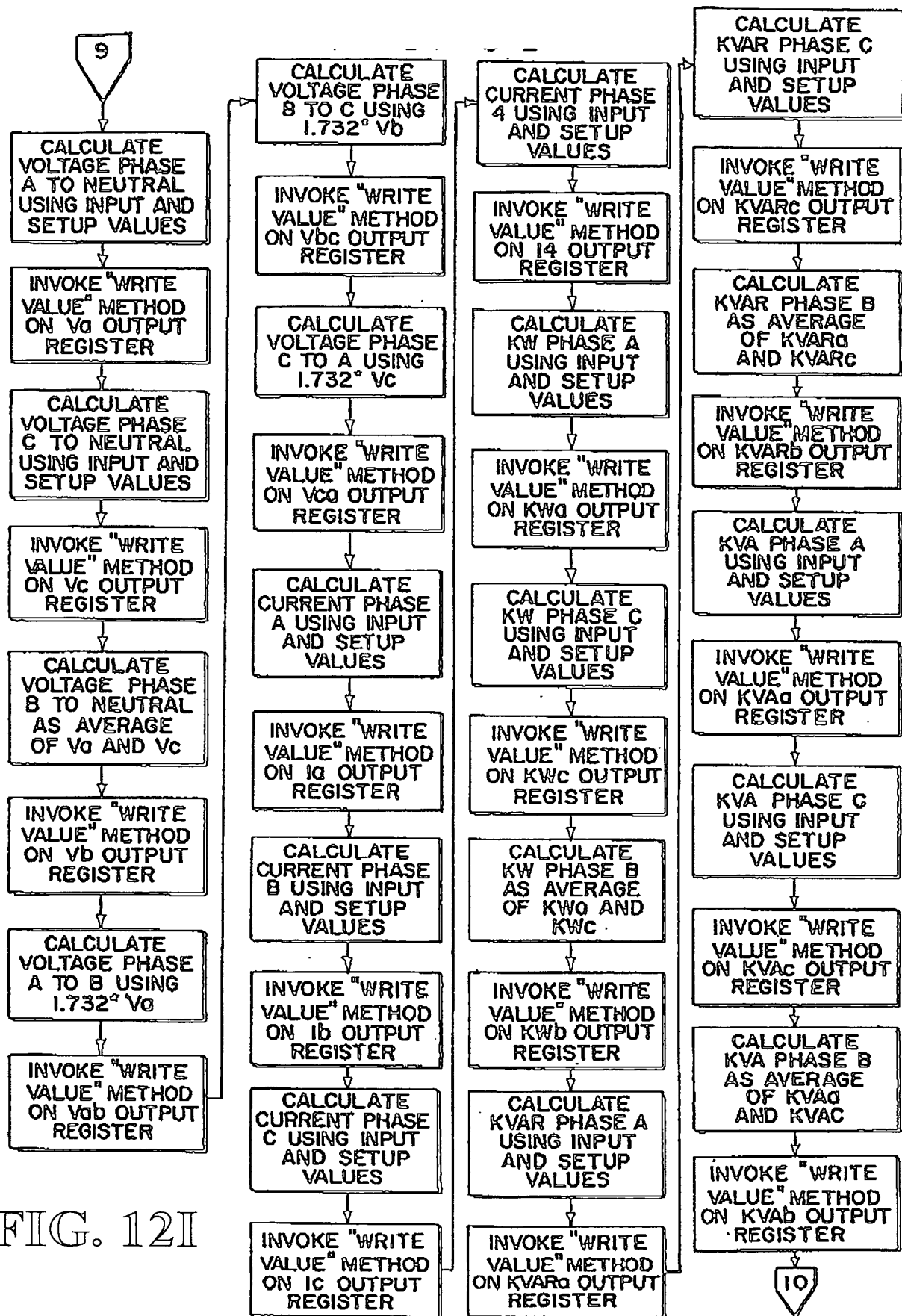


FIG. 12J

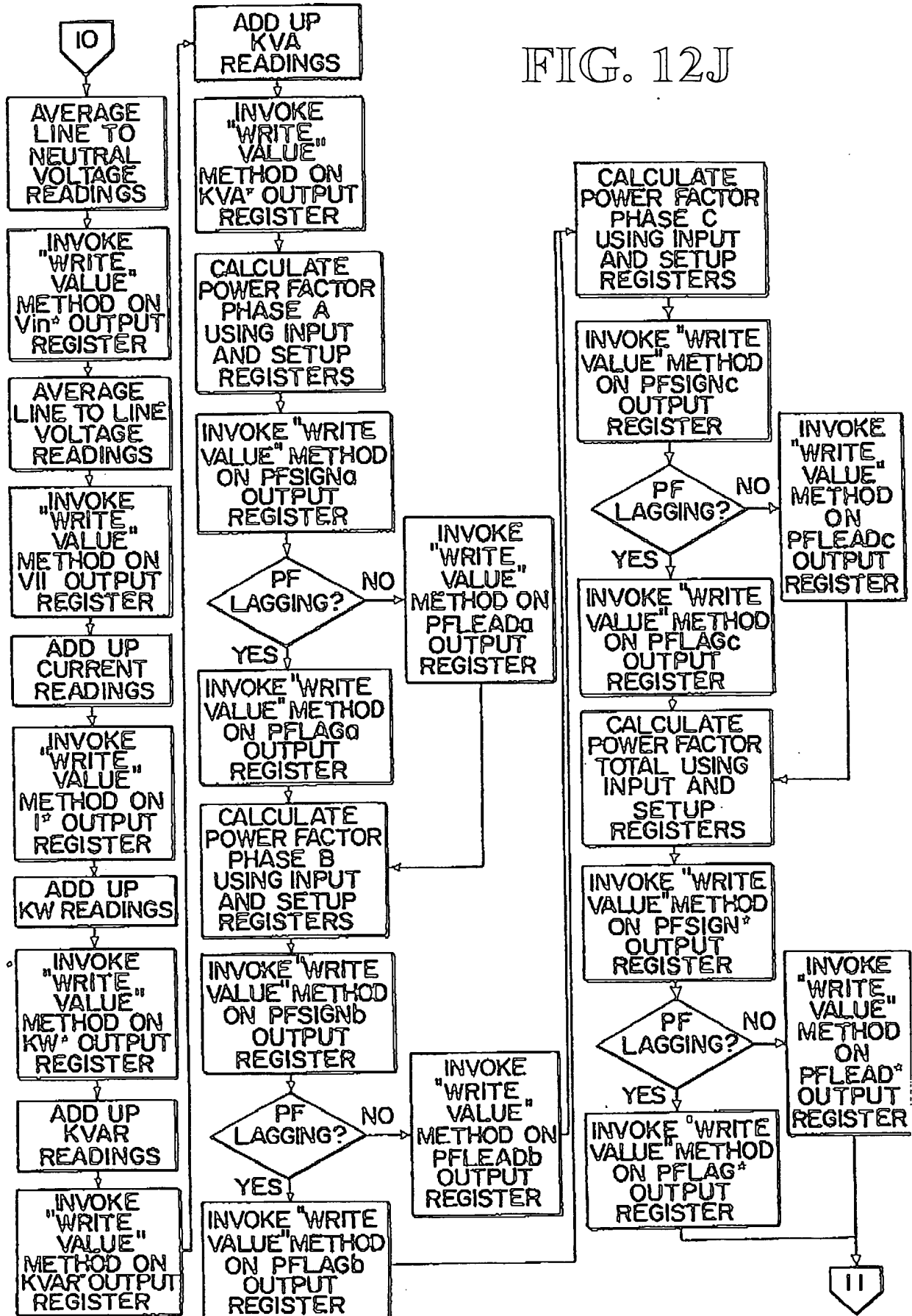


FIG. 12K

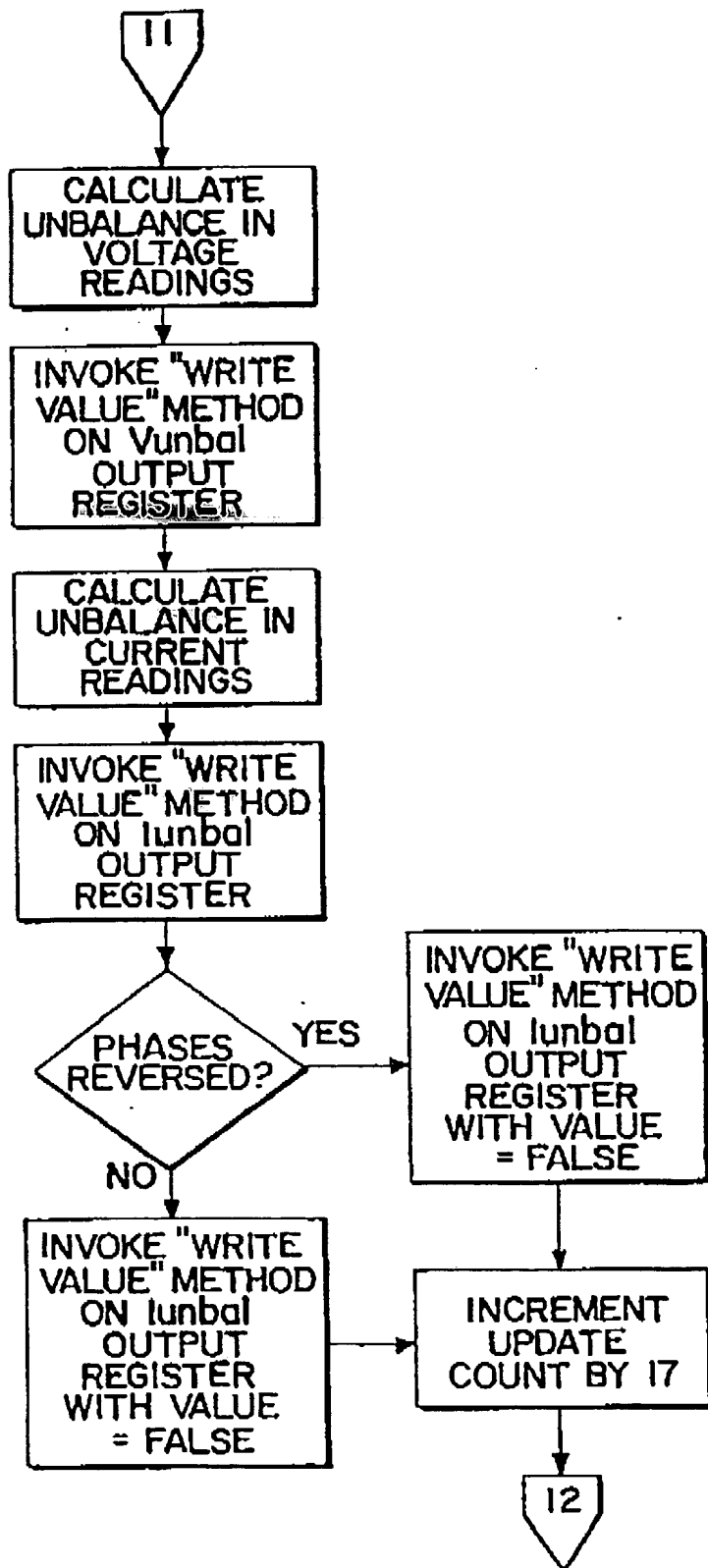


FIG. 12L

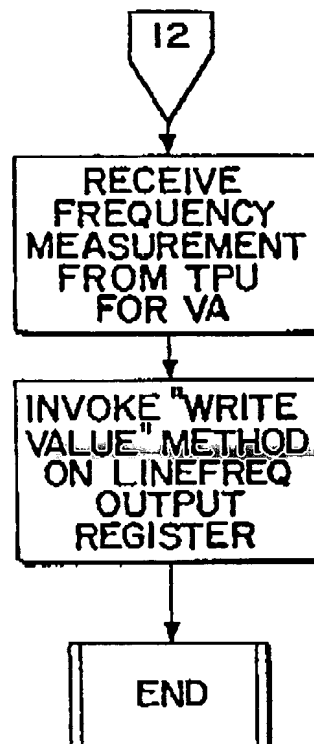


FIG. 13

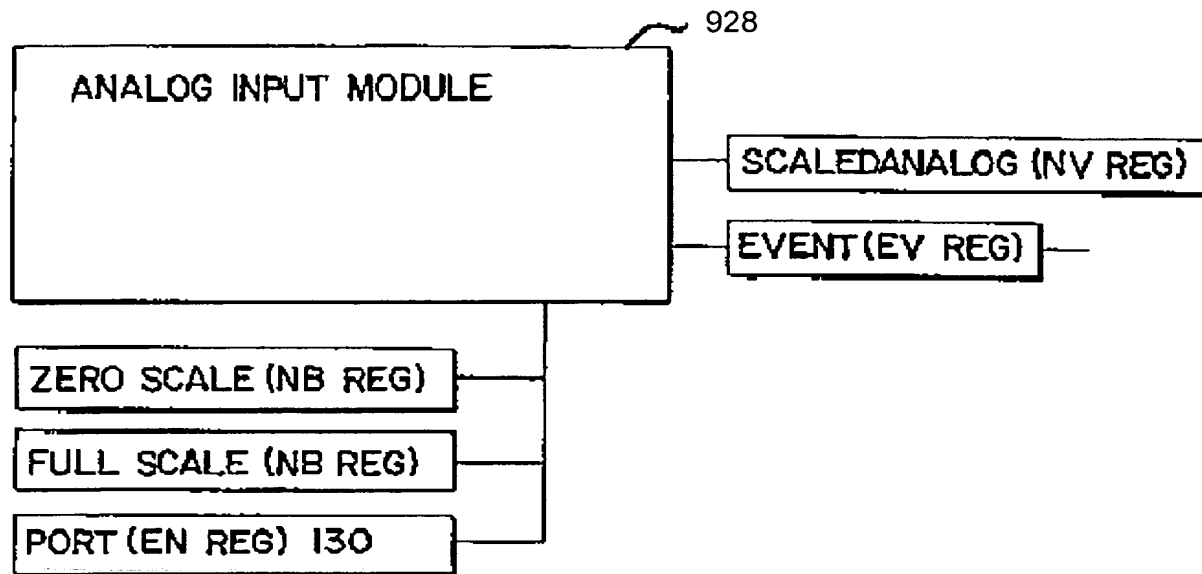


FIG. 14

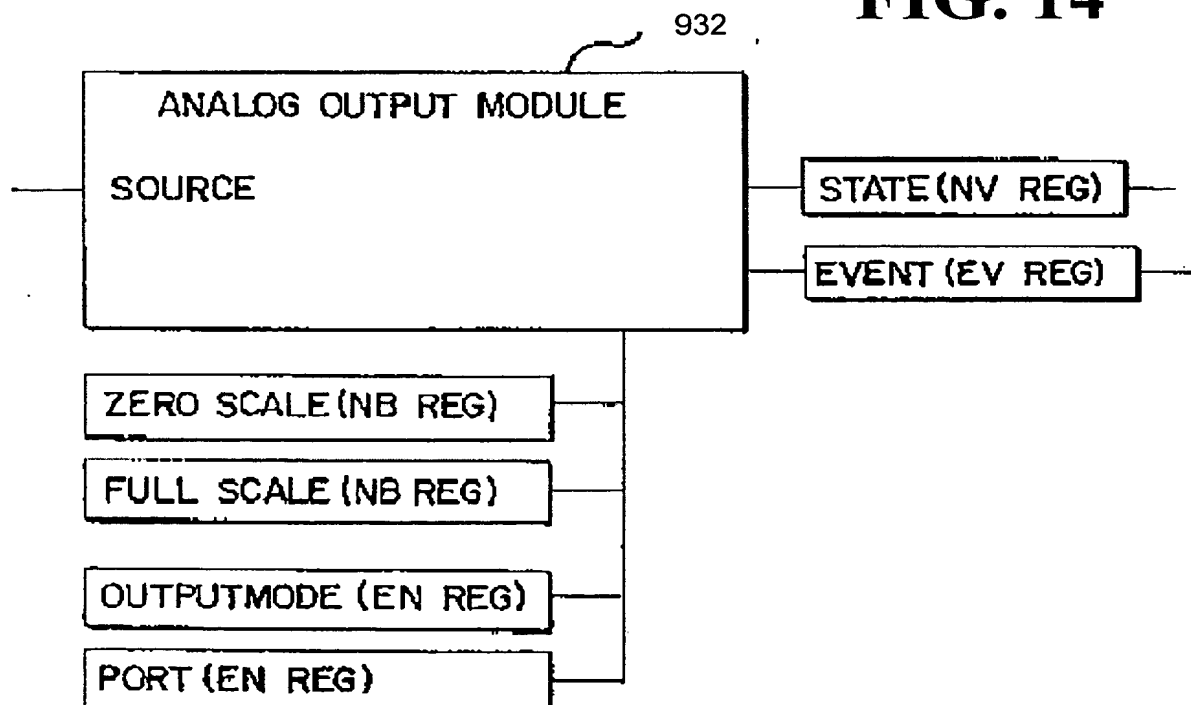


FIG. 13A

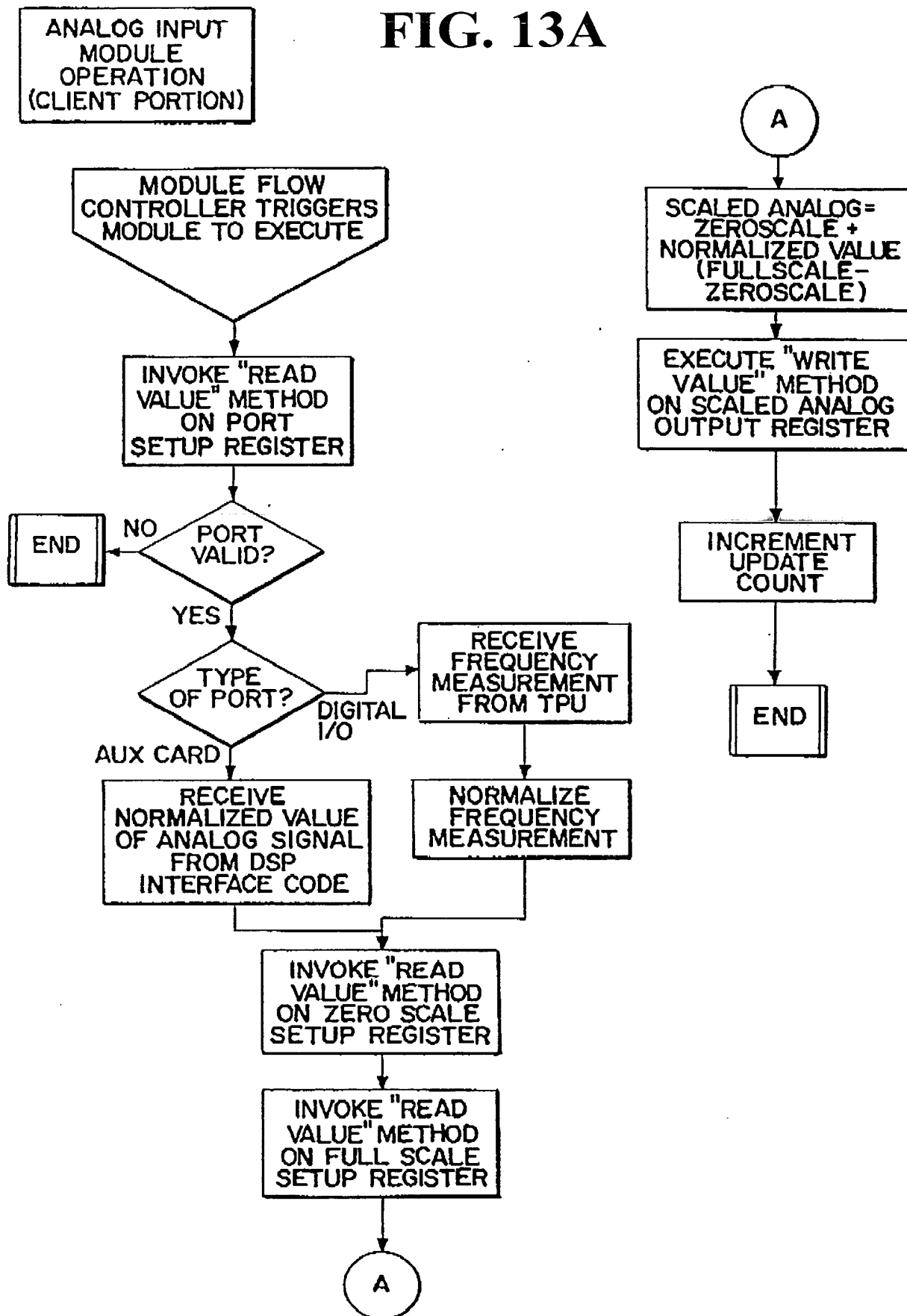


FIG. 14A

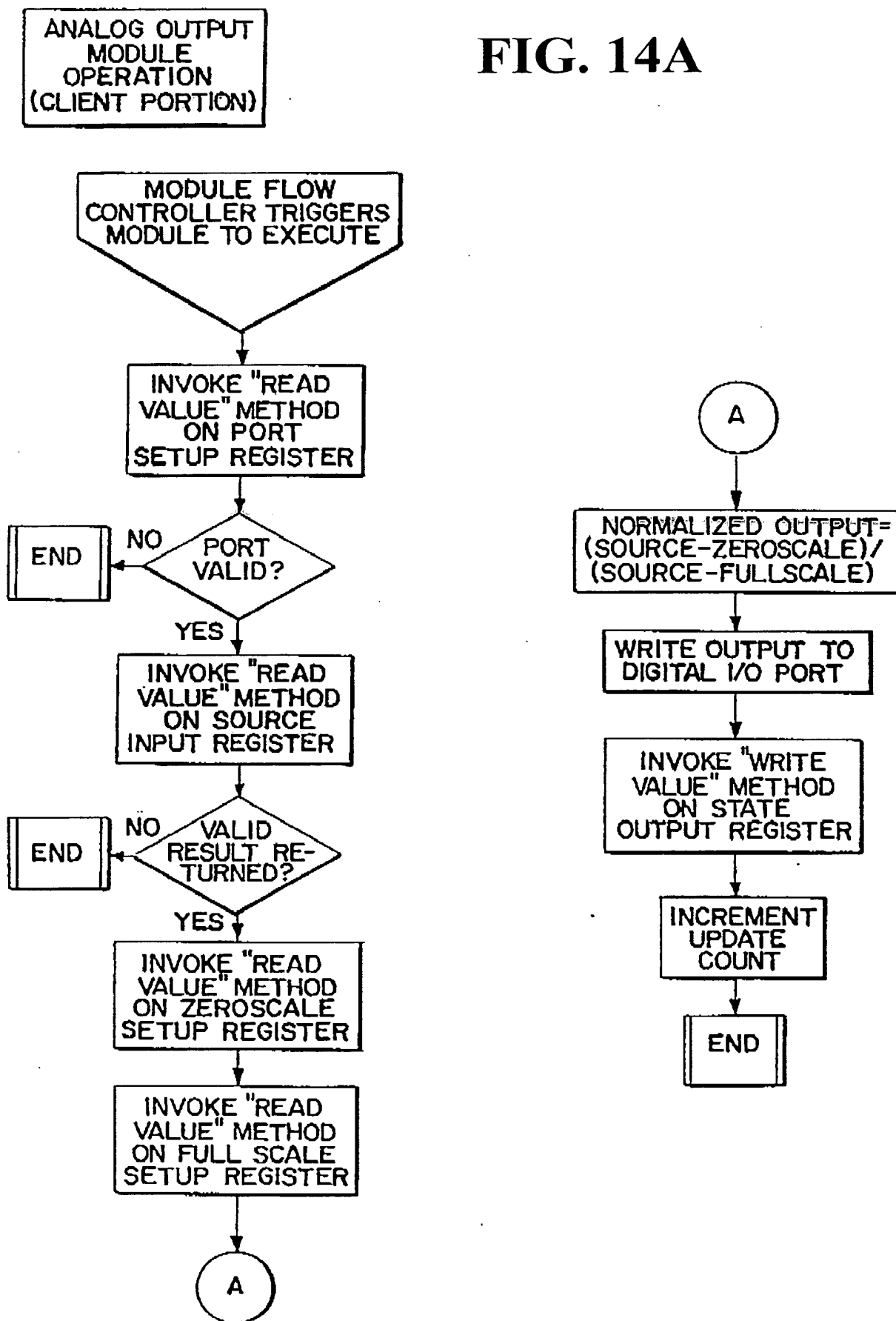


FIG. 15

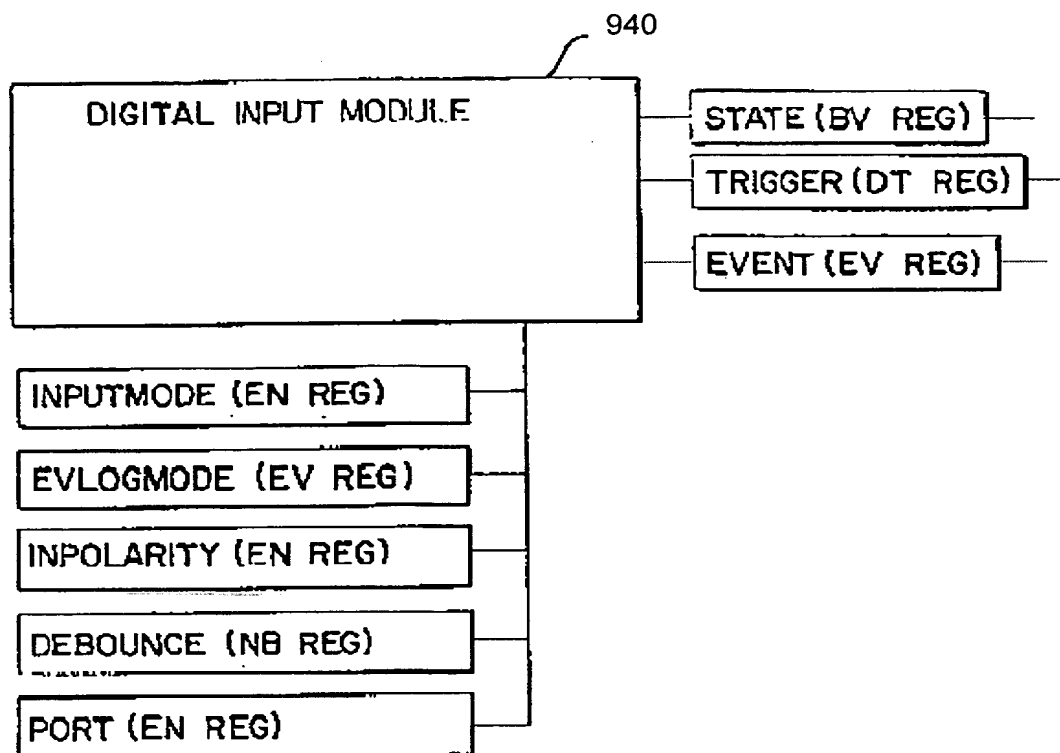


FIG. 16

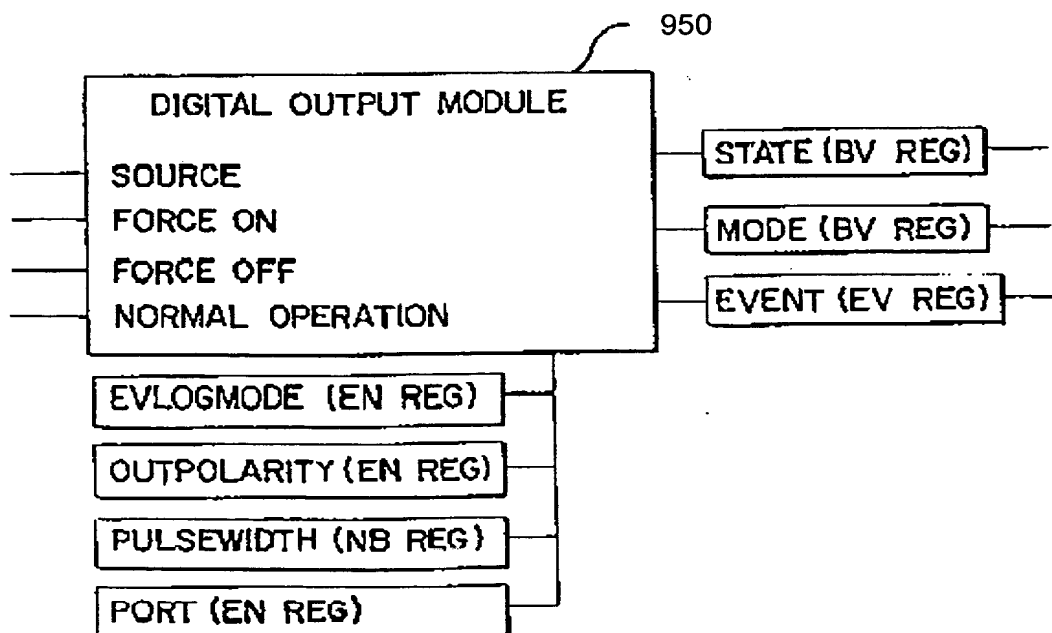


FIG. 15A

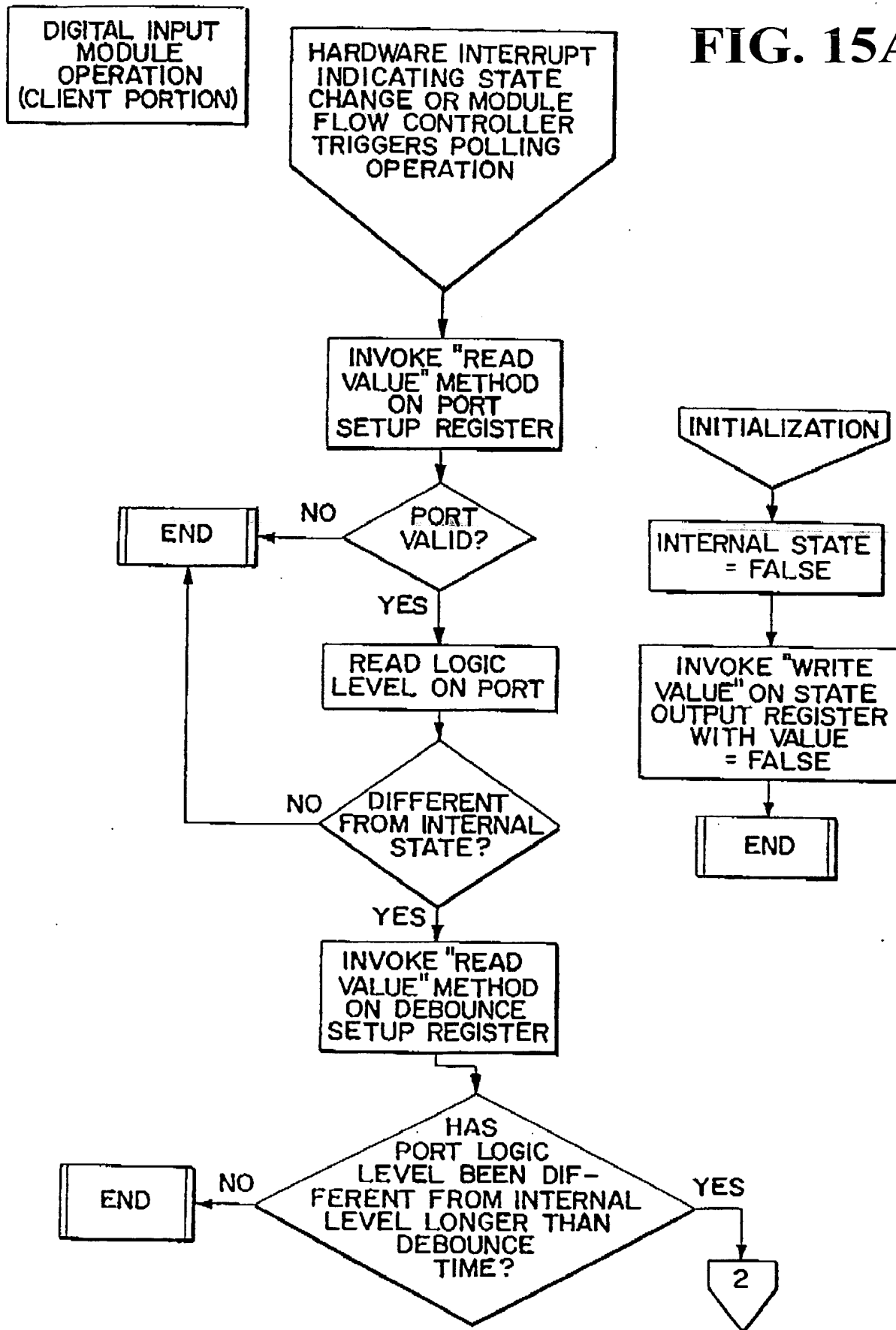


FIG. 15B

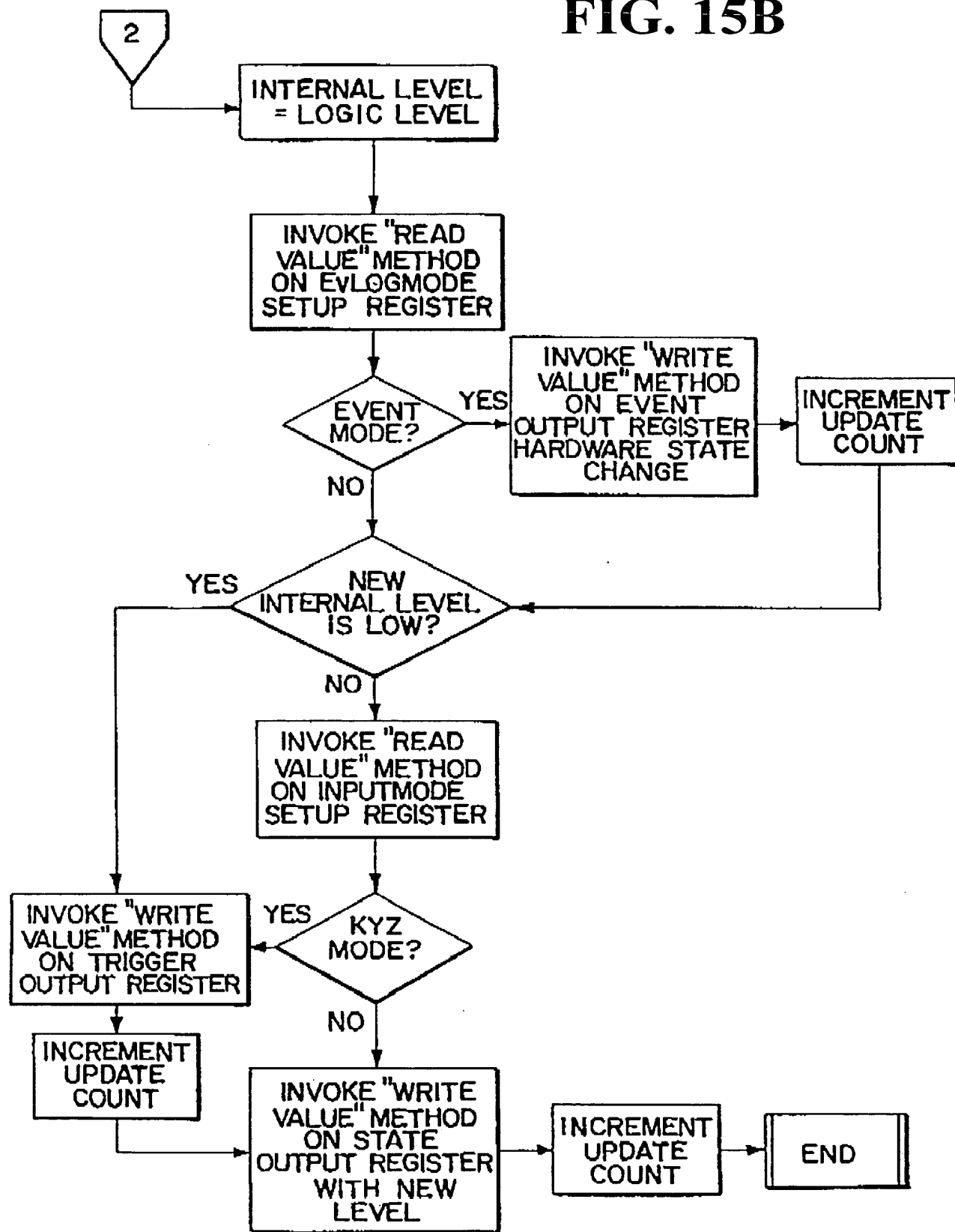


FIG. 16A

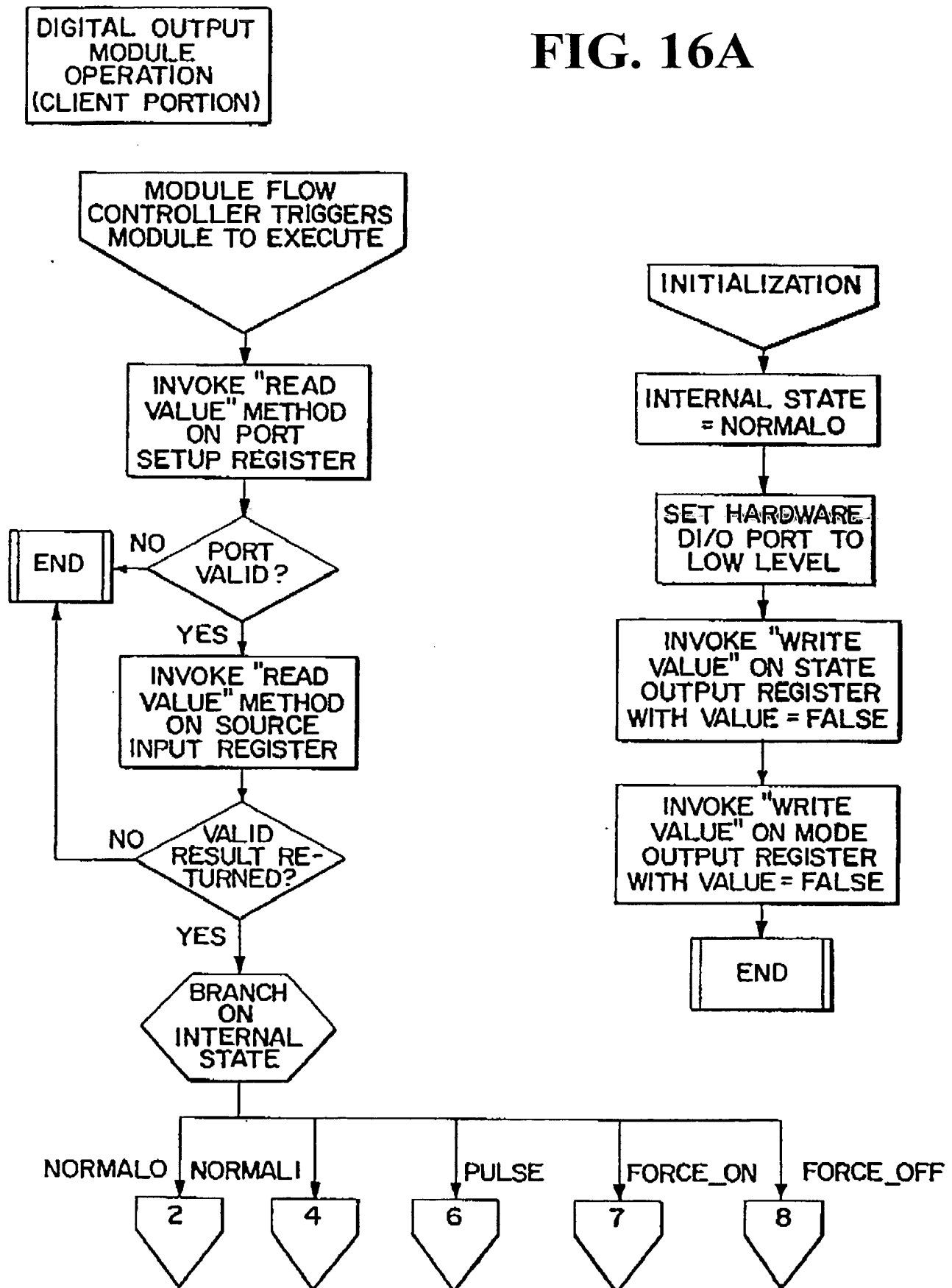


FIG. 16B

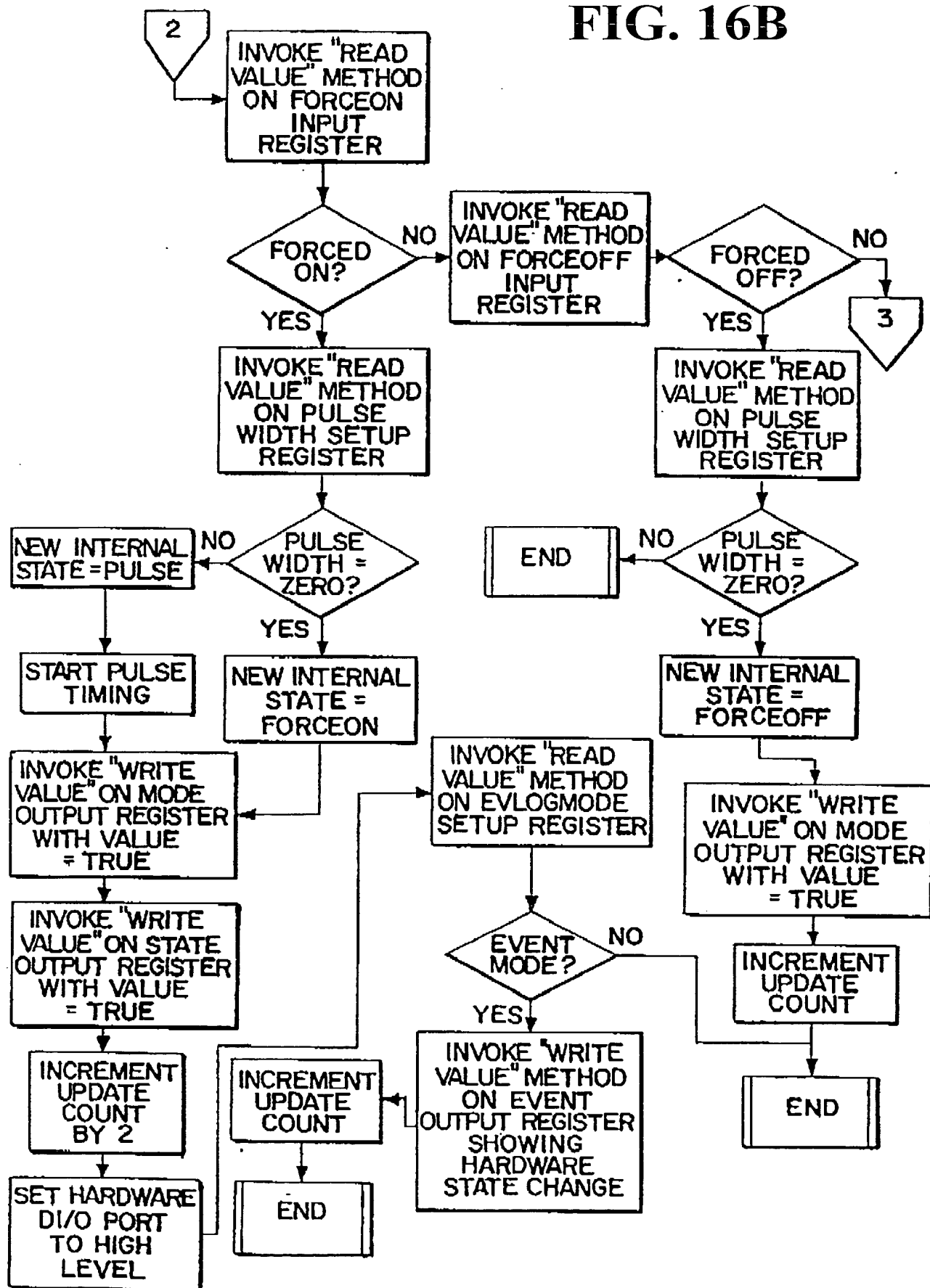


FIG. 16C

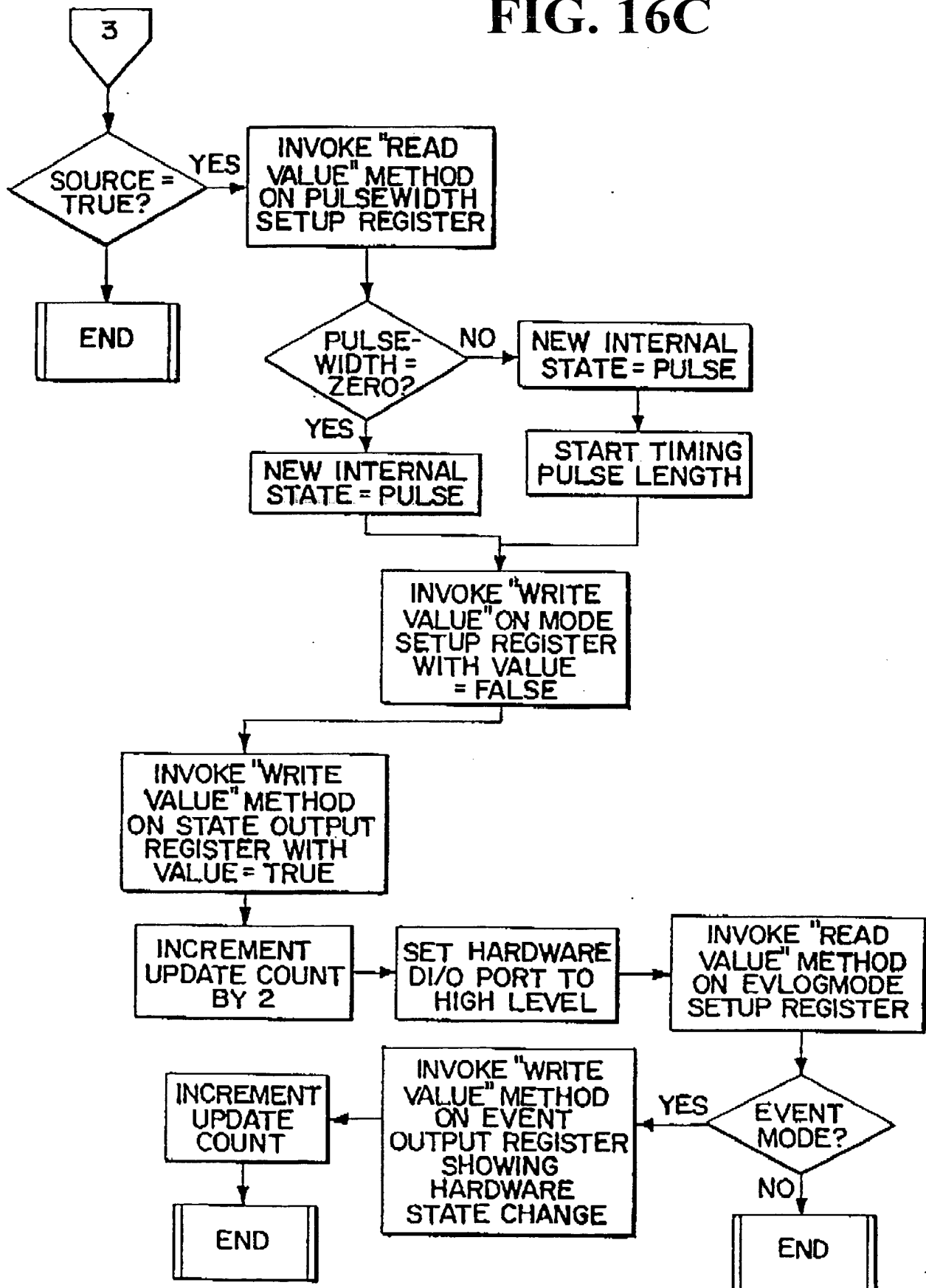


FIG. 16D

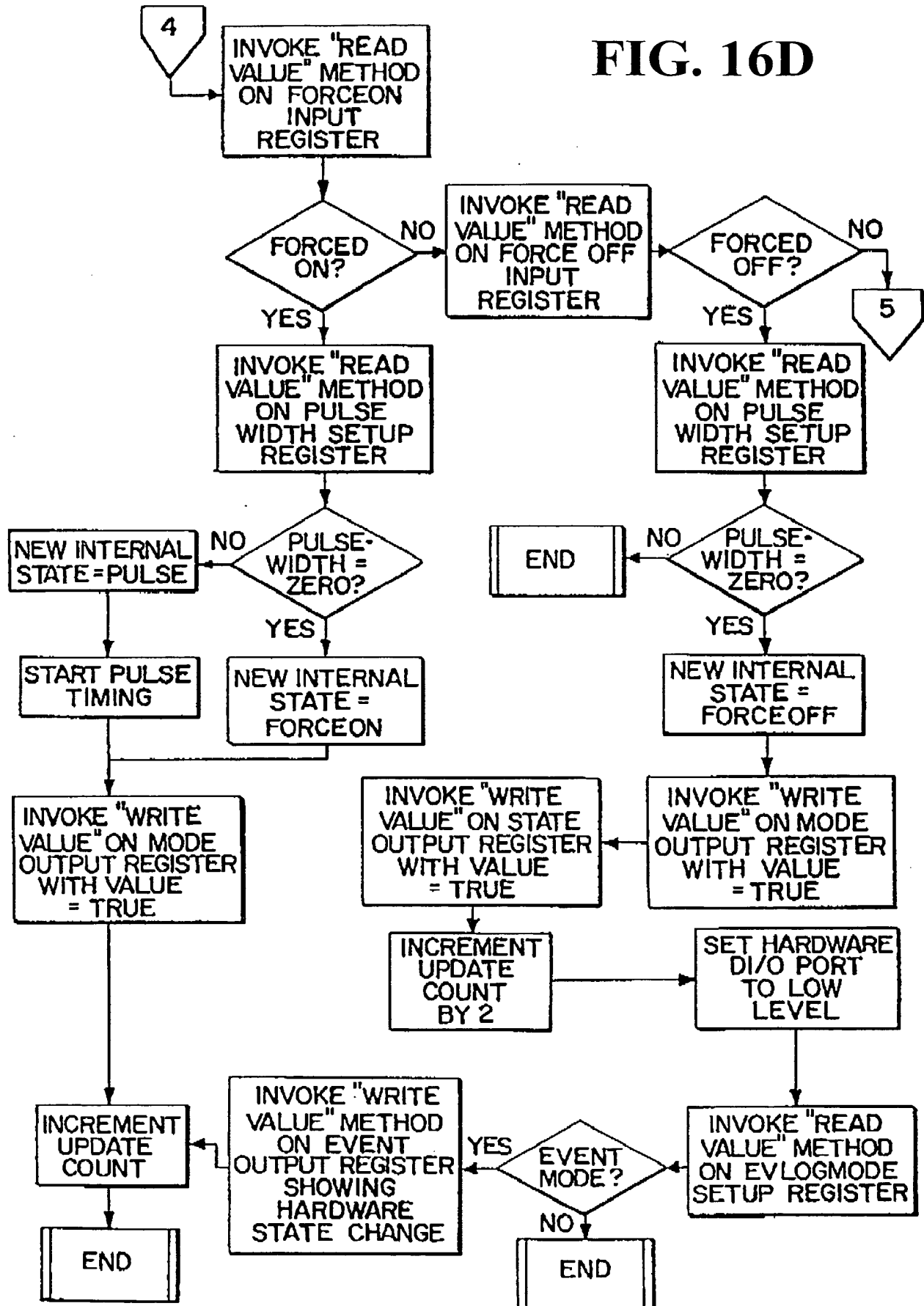


FIG. 16E

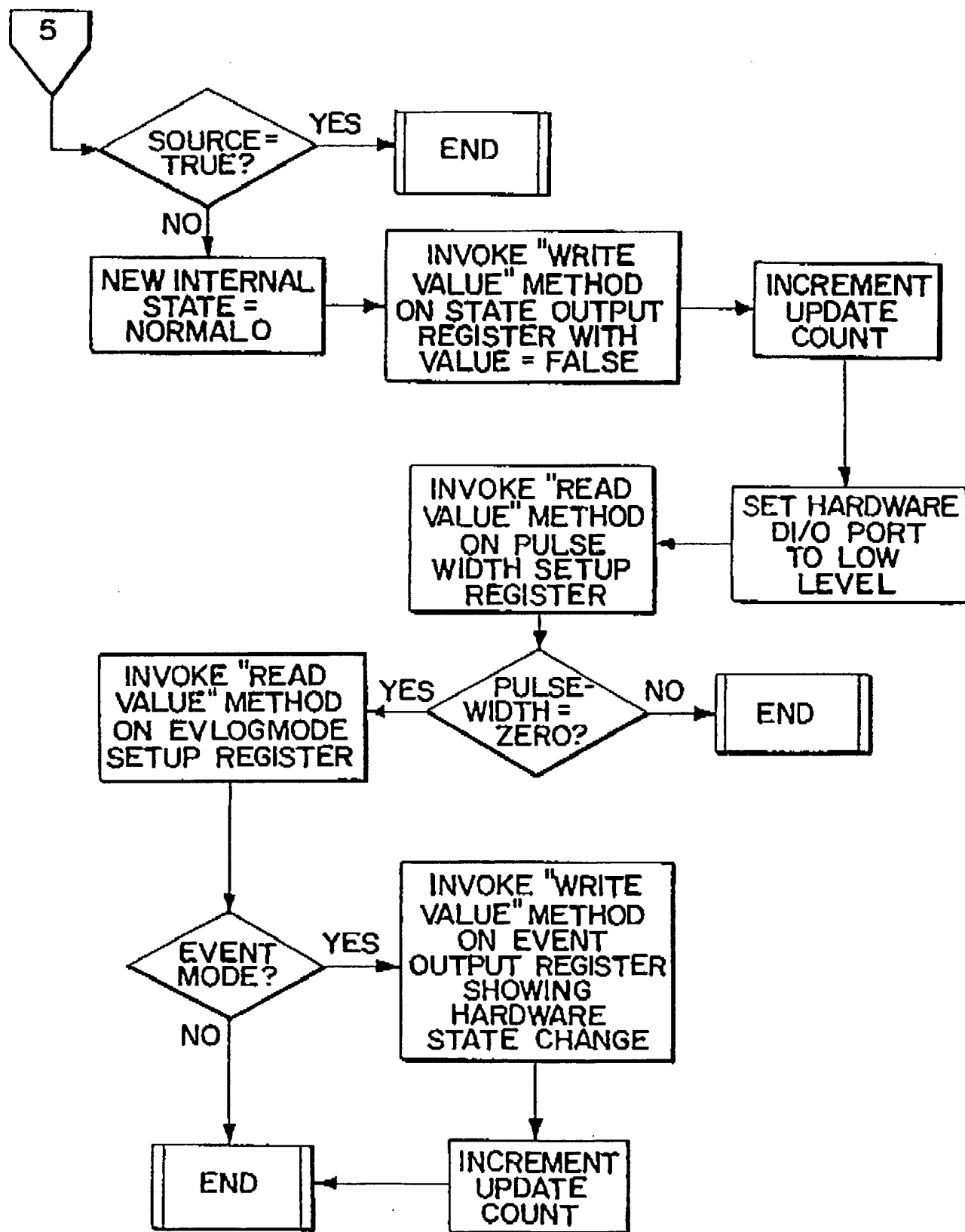


FIG. 16F

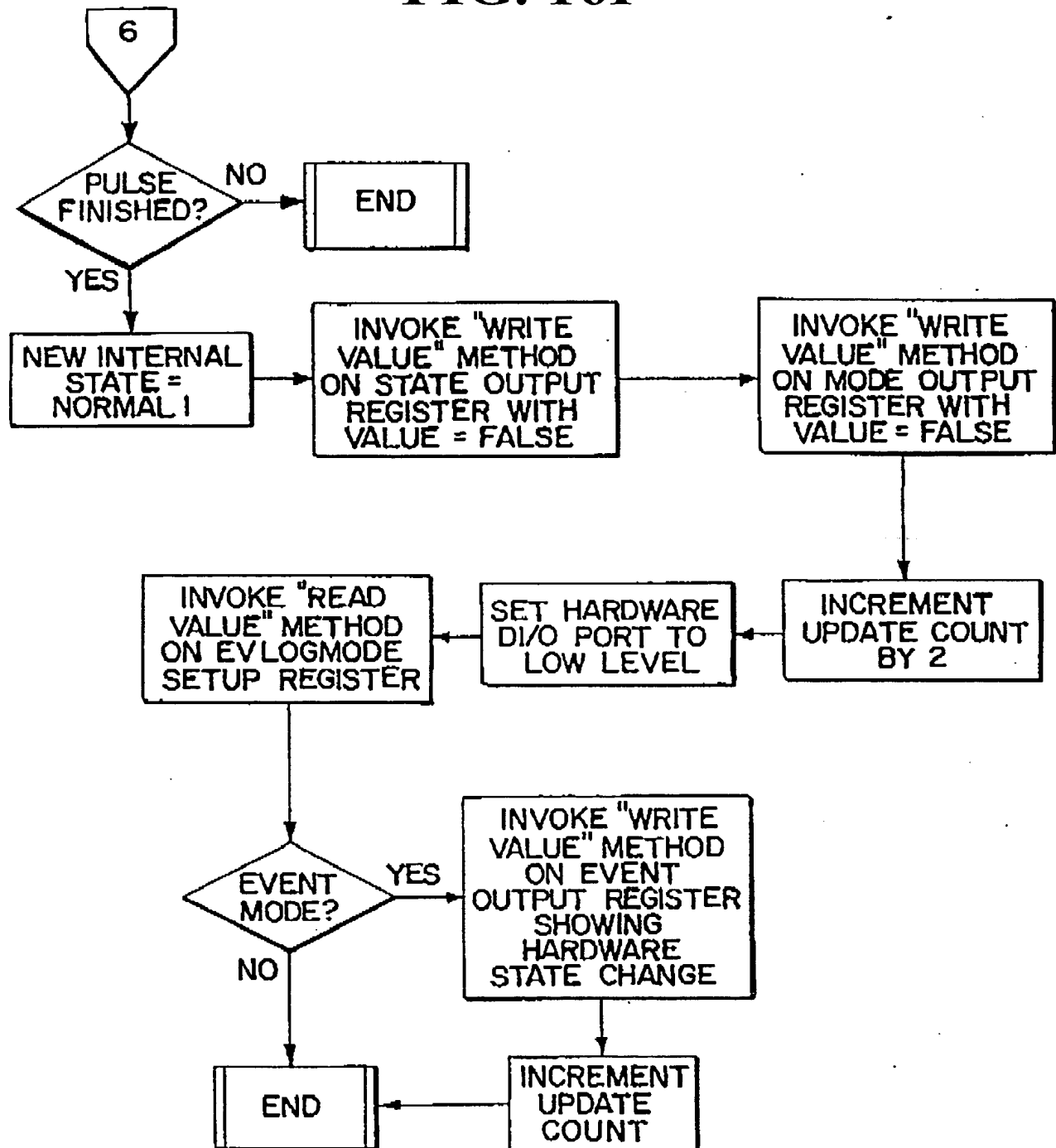


FIG. 16G

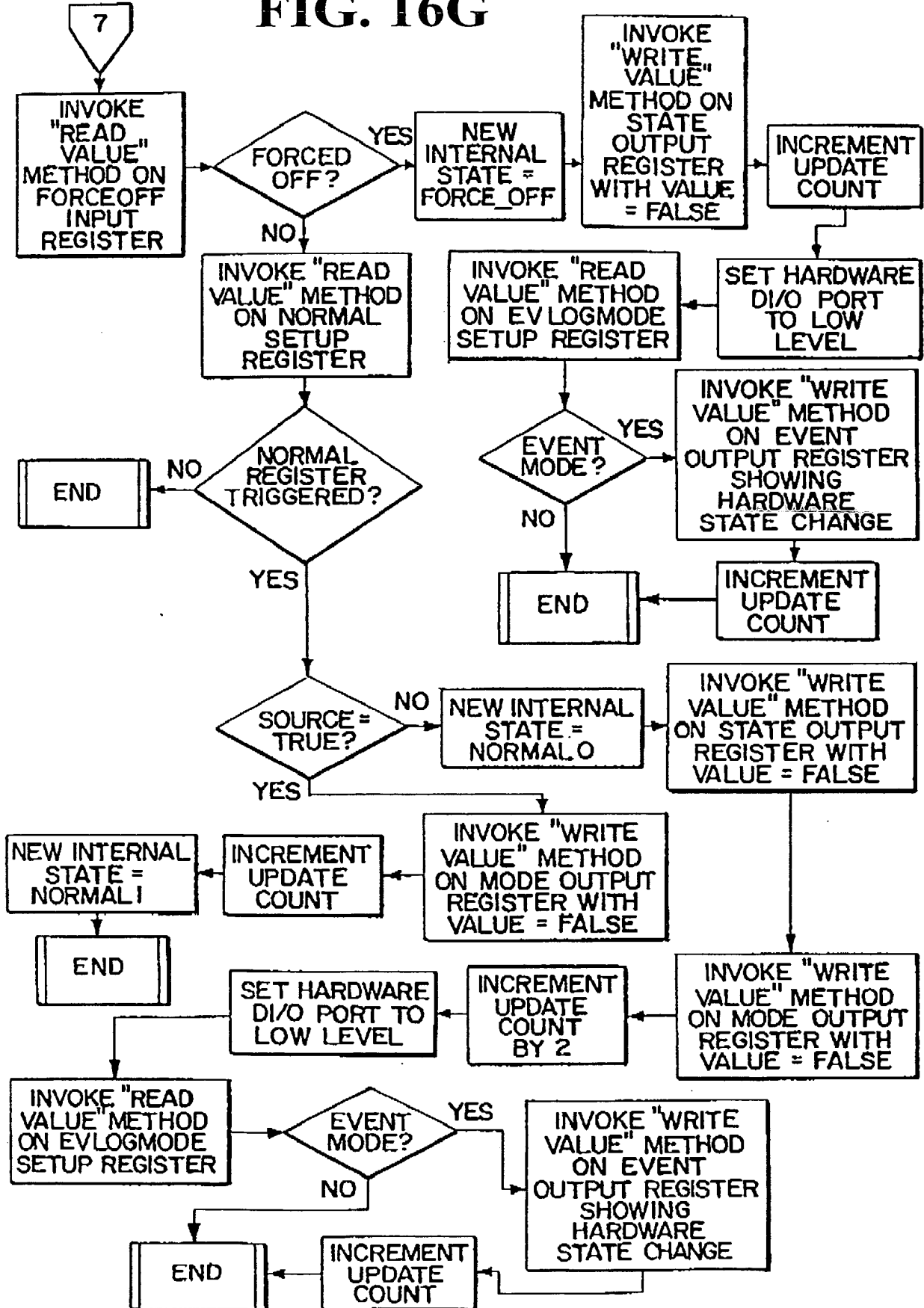


FIG. 16H

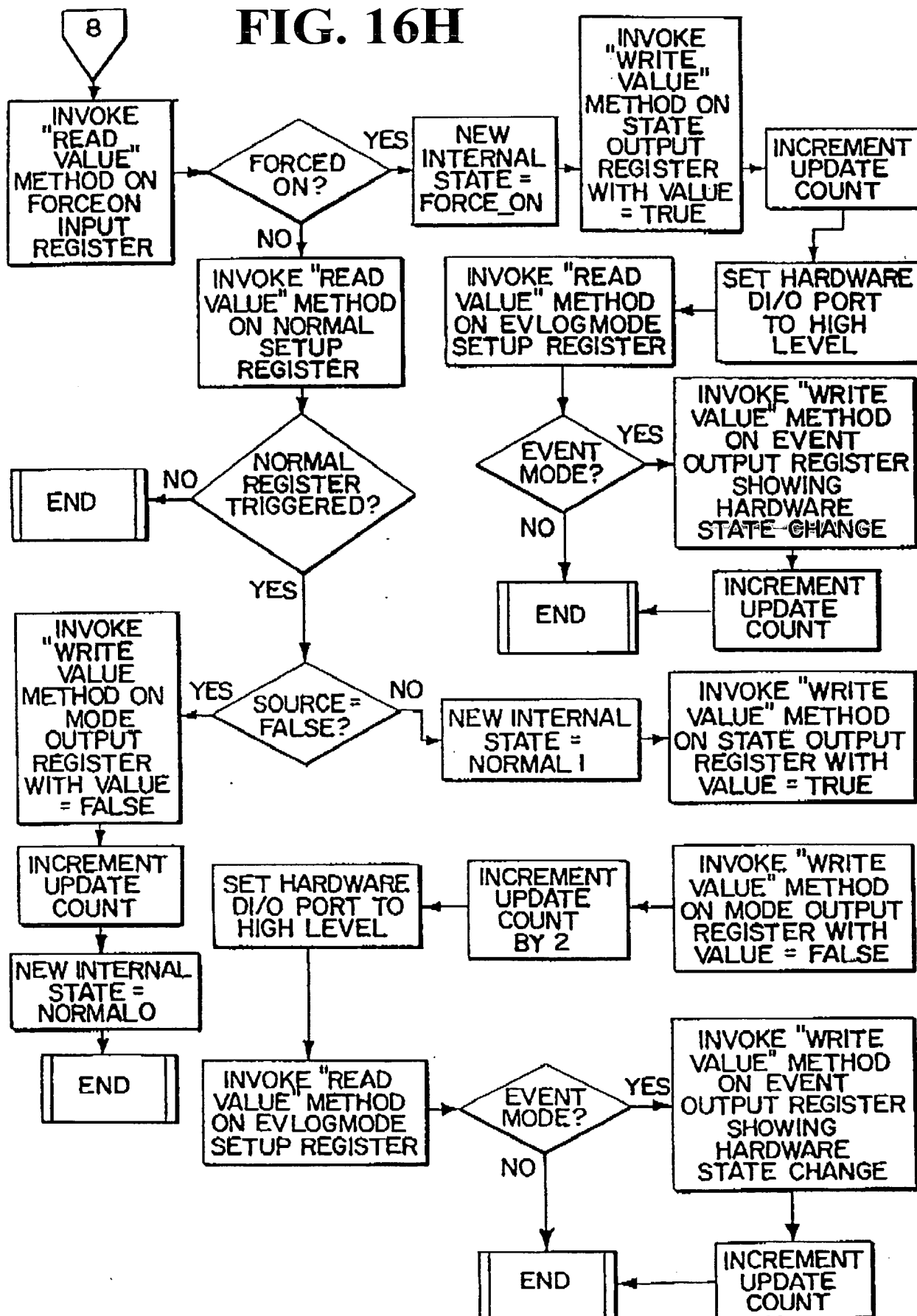


FIG. 17

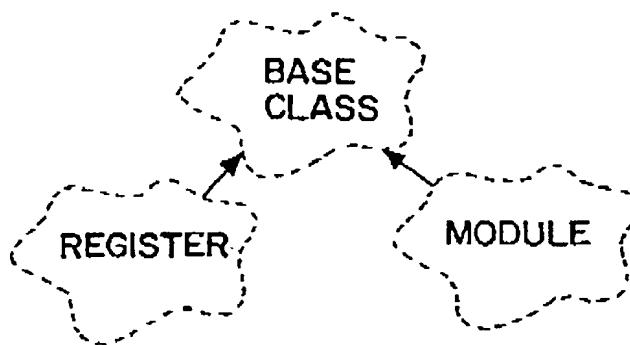


FIG. 17A

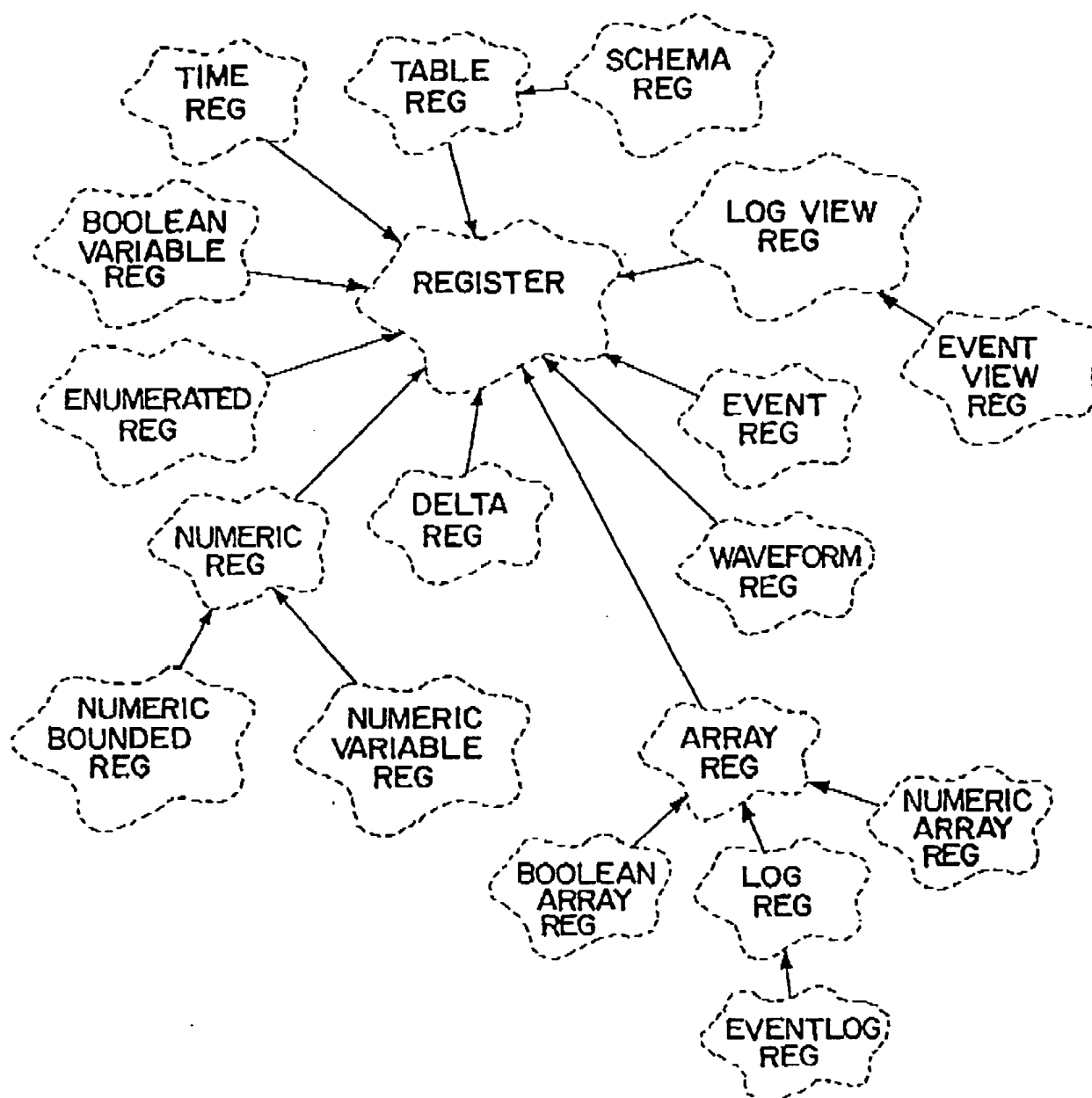


FIG. 17B

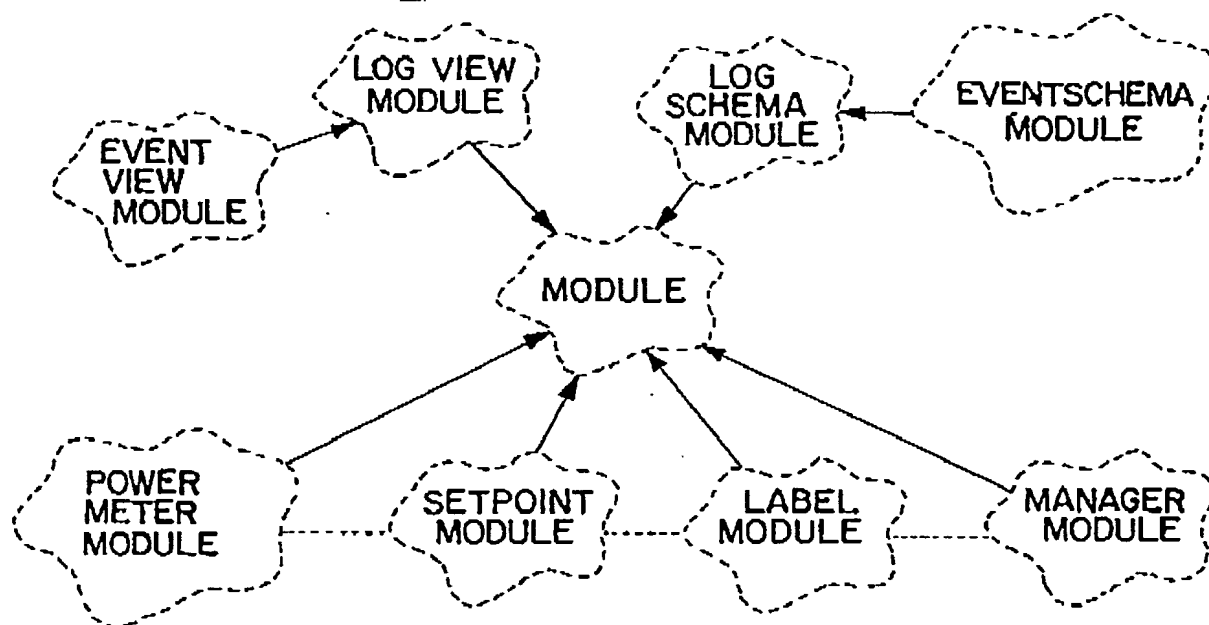
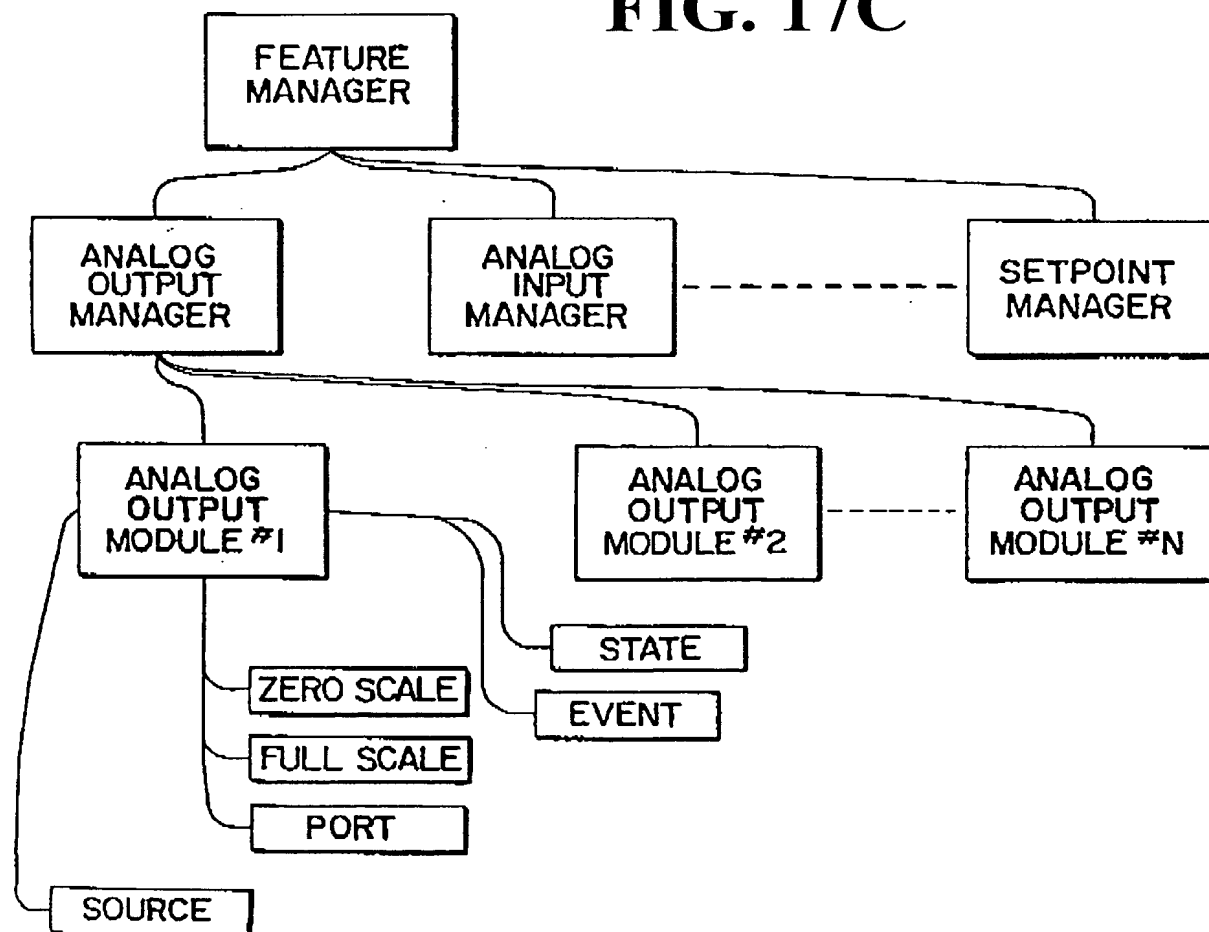


FIG. 17C



MODULE HANDLE

MODULE

- CLASS(CL)
- NAME(S)
- LABEL(S)
- METHODSECURITY(M,SE)
- ...
- METHODSECURITY(M,SE)
- OWNERS(AH)

ACCESSED USING BASE CLASS METHODS

INPUT HANDLES (AH)

- SETUP HANDLES (AH)
- SETUPCOUNTER(C)
- UPDATECOUNTER(C)
- UPDATEPERIOD(N)
- MODULE.FSECURITY(SE)

ACCESSED USING MODULE METHODS

OUTPUT HANDLES

- REGISTER1(RXX)
- REGISTERN(RXX)

ACCESSED USING REGISTER METHODS

REGISTERS ACCESSED USING REGISTER METHODS

- REGISTER(RXX) OR MODULE
- REGISTERN(RXX) OR MODULE

MODULES ACCESSED USING MODULE METHODS

A block diagram of a system architecture. A central rectangular block is labeled "MODULE". To the left of the module, there are two rectangular blocks, each labeled "REGISTER". Dashed arrows point from these registers to the left side of the module. The top register is labeled "863a" and the bottom register is labeled "863n". A bracket groups these two registers and is labeled "869n". To the right of the module, there are two rectangular blocks, each labeled "REGISTER". Dashed arrows point from the right side of the module to these registers. The top register is labeled "864a" and the bottom register is labeled "864n". A bracket groups these two registers and is labeled "870n". Below the module, there are two rectangular blocks, each labeled "REGISTER". Dashed arrows point from these registers to the bottom of the module. The top register is labeled "867a" and the bottom register is labeled "867n". A bracket groups these two registers and is labeled "872n". Above the bottom registers, there is a label "SETUP REGISTERS". A bracket groups the two bottom registers and is labeled "872a". A bracket groups the two bottom registers and is labeled "861".

FIG. 19A

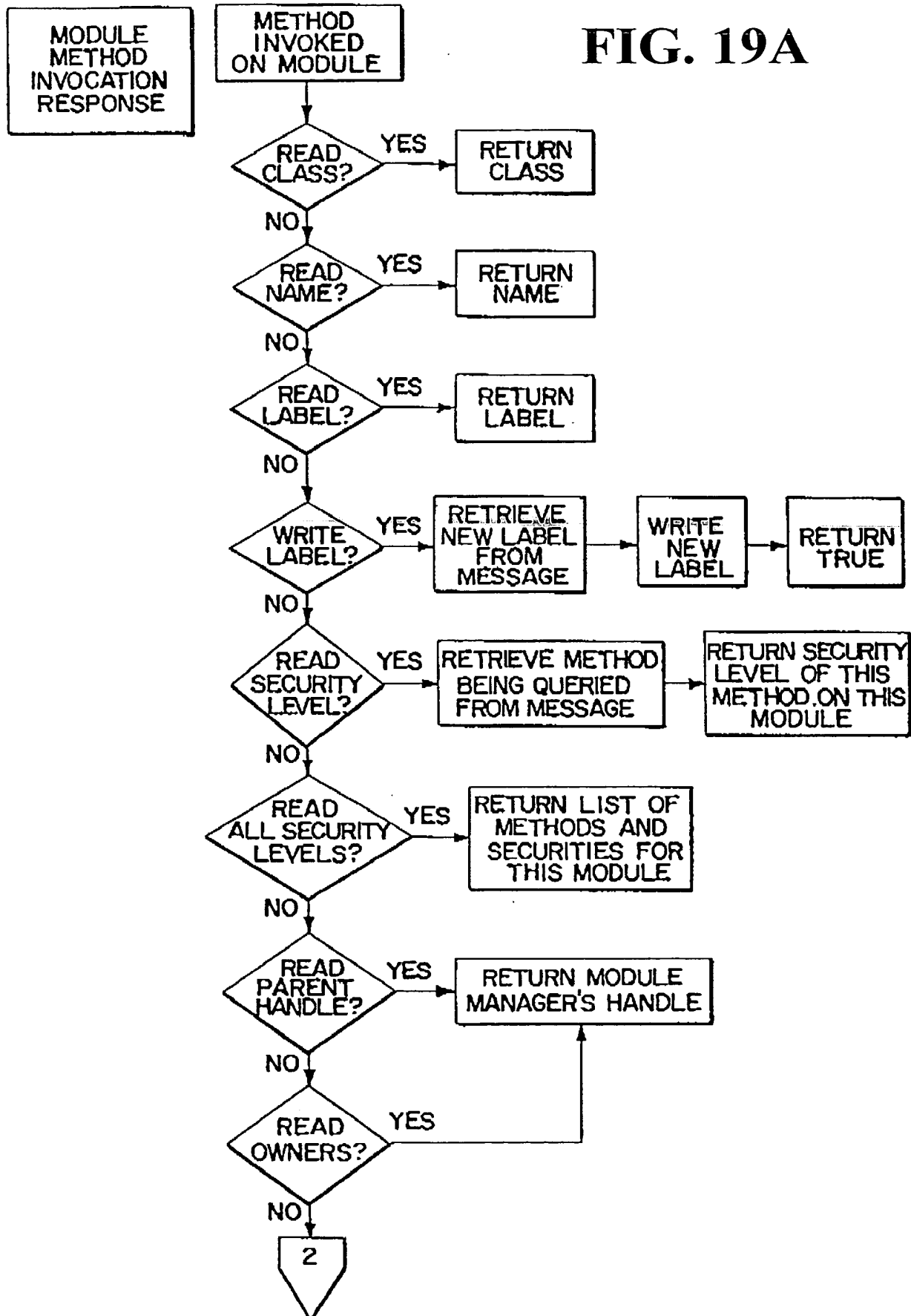


FIG. 19B

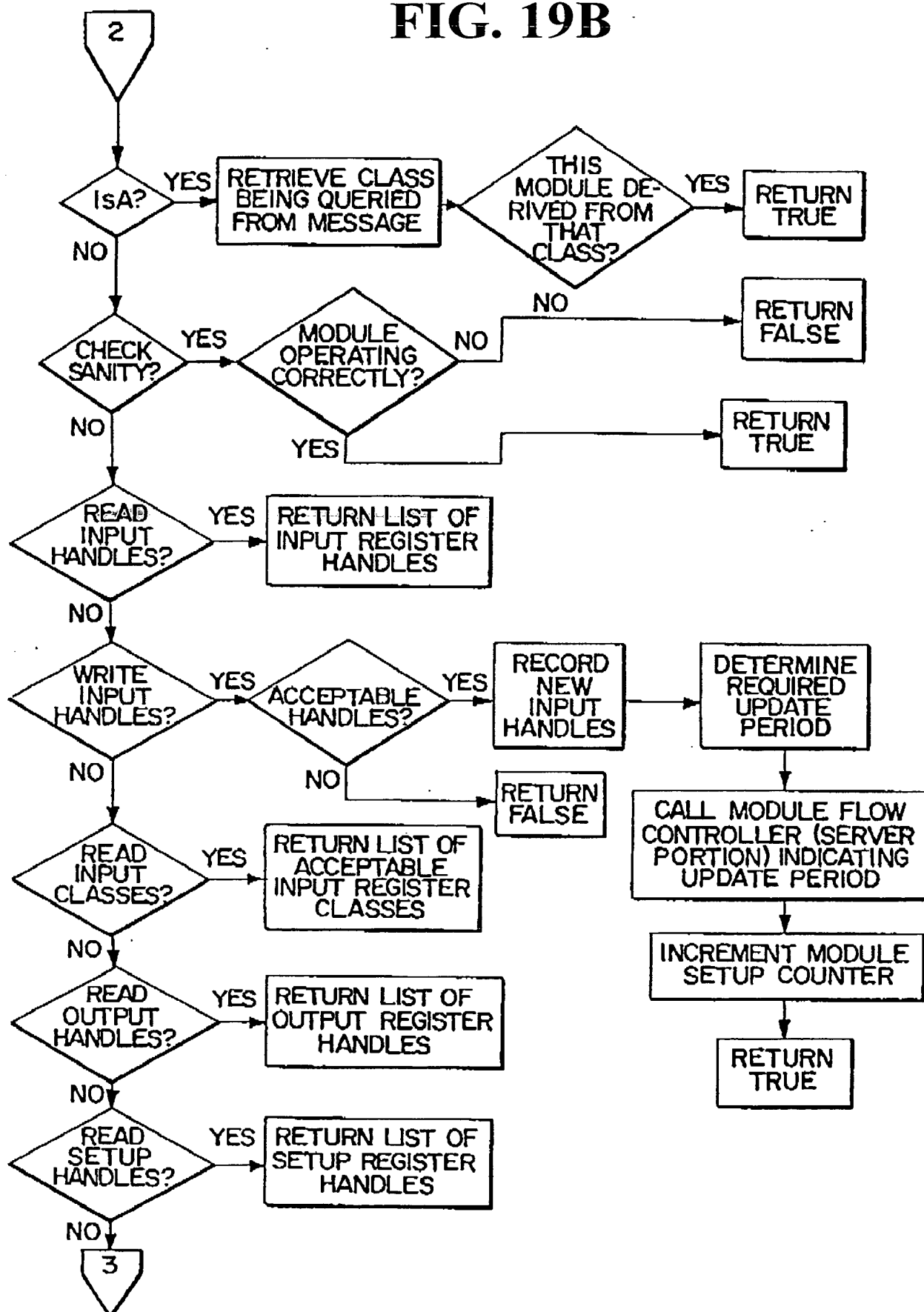


FIG. 19C

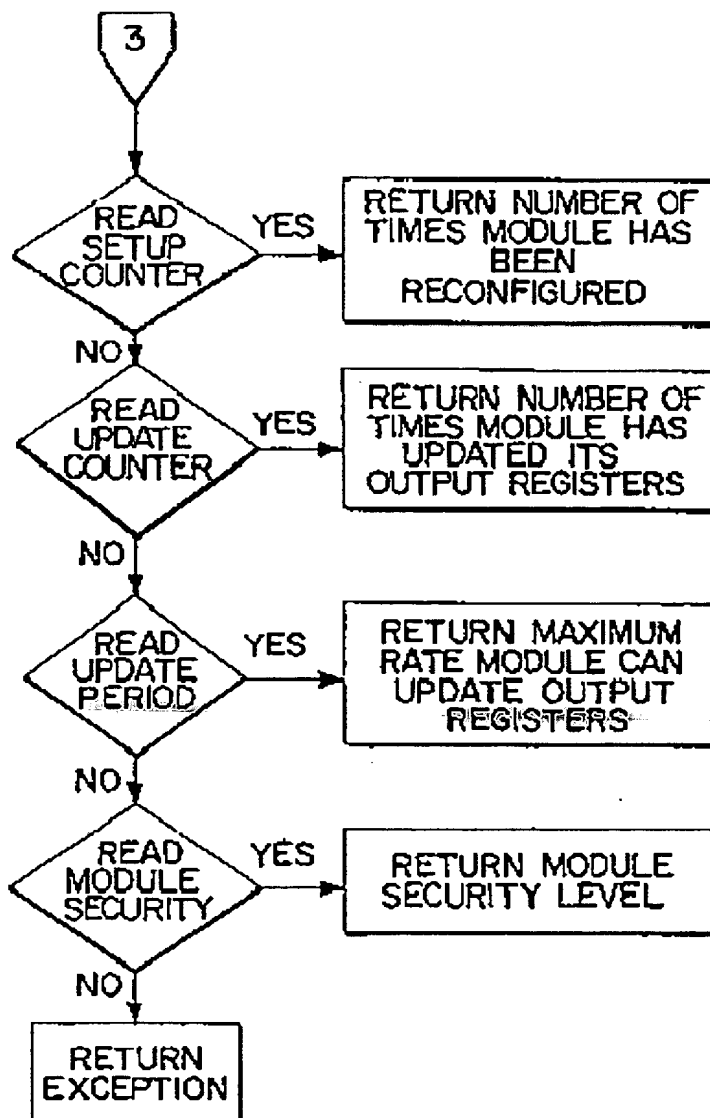


FIG. 20

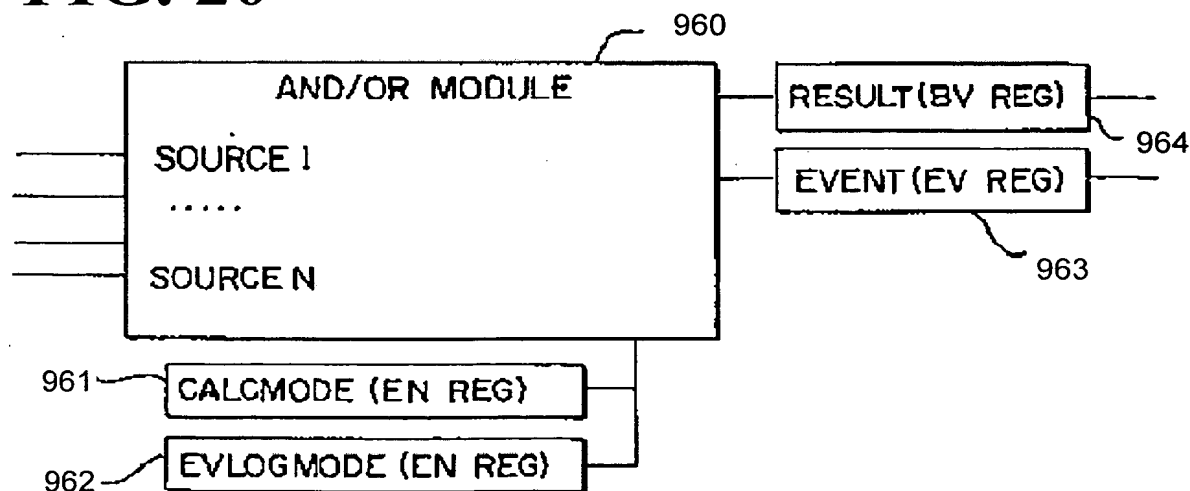


FIG. 20A

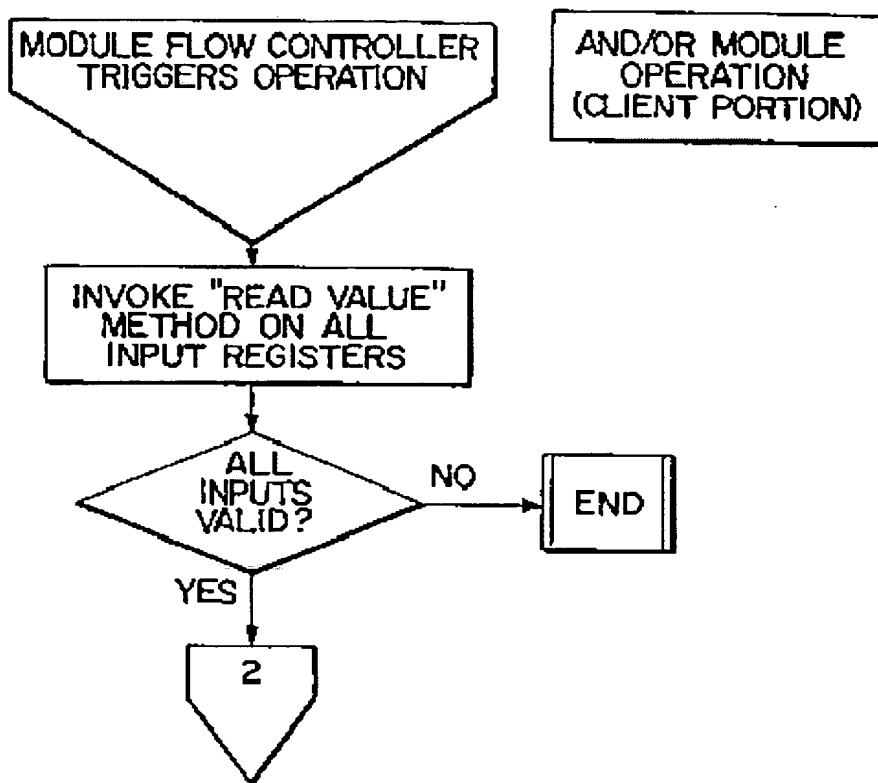


FIG. 21

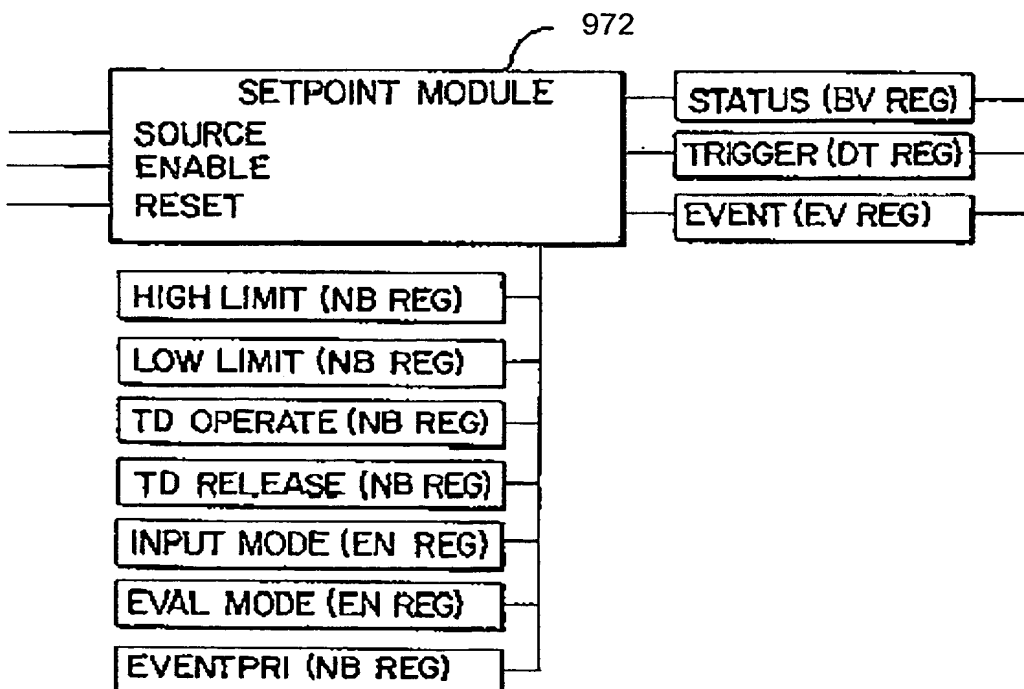


FIG. 20B

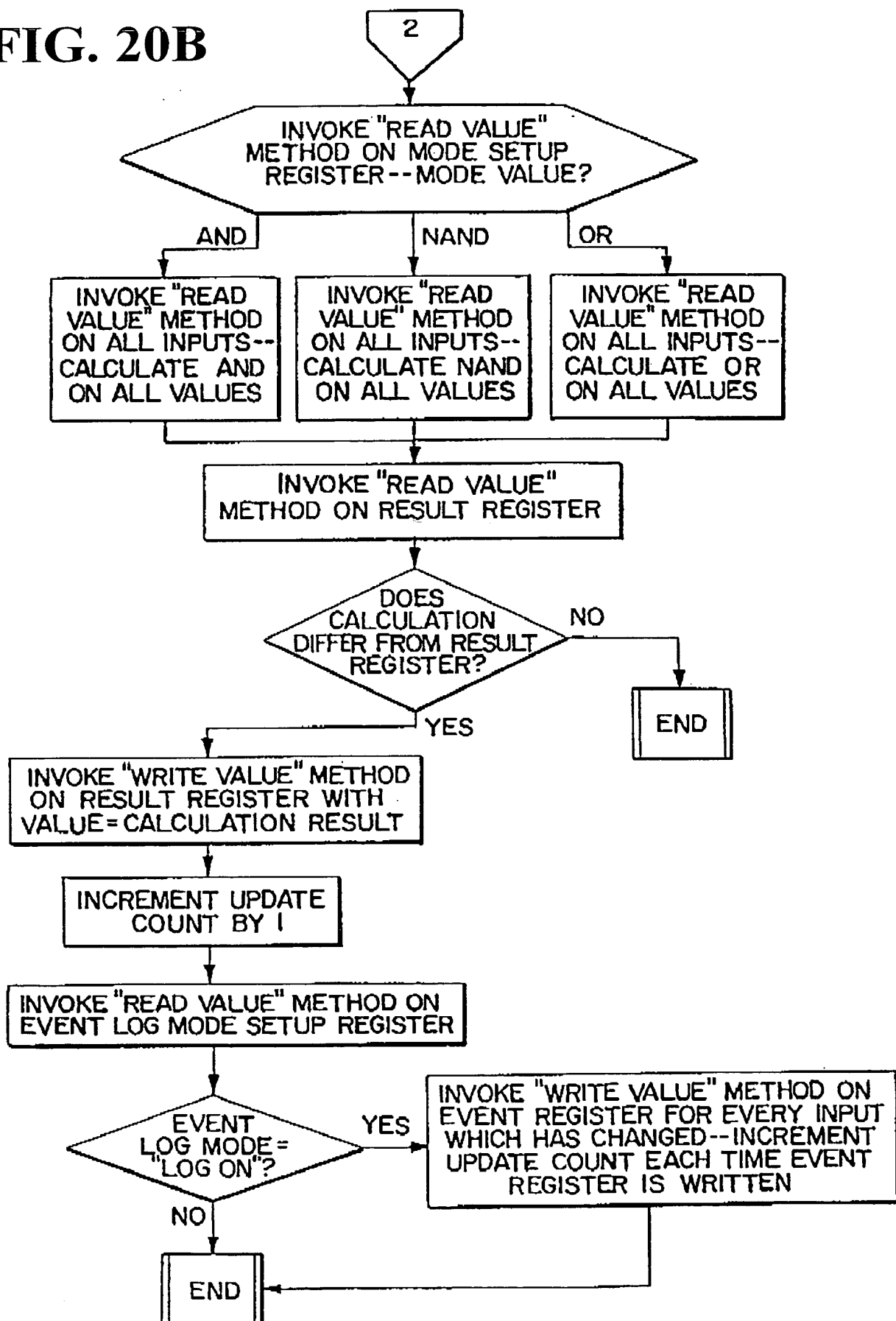


FIG. 21A

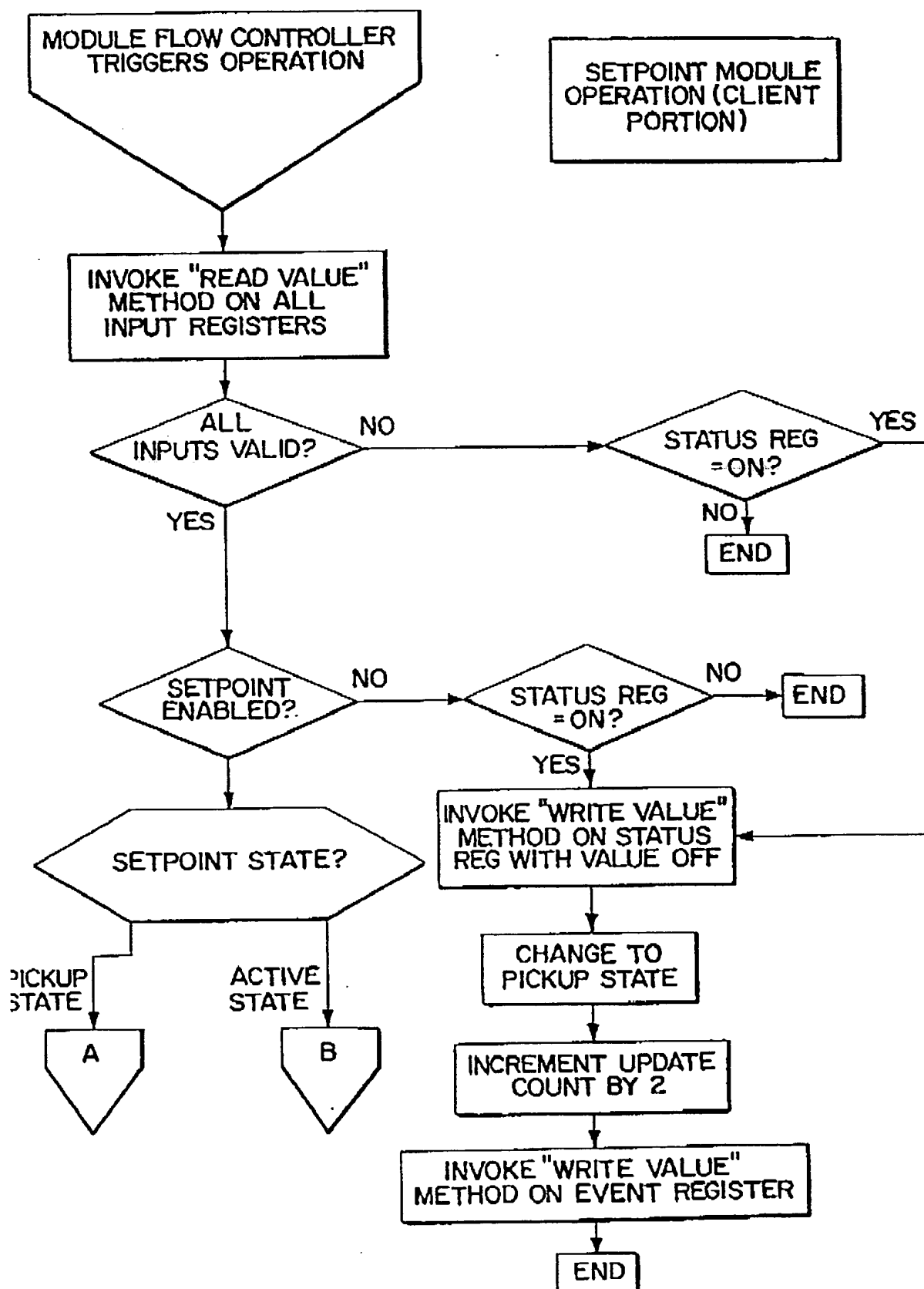


FIG. 21B

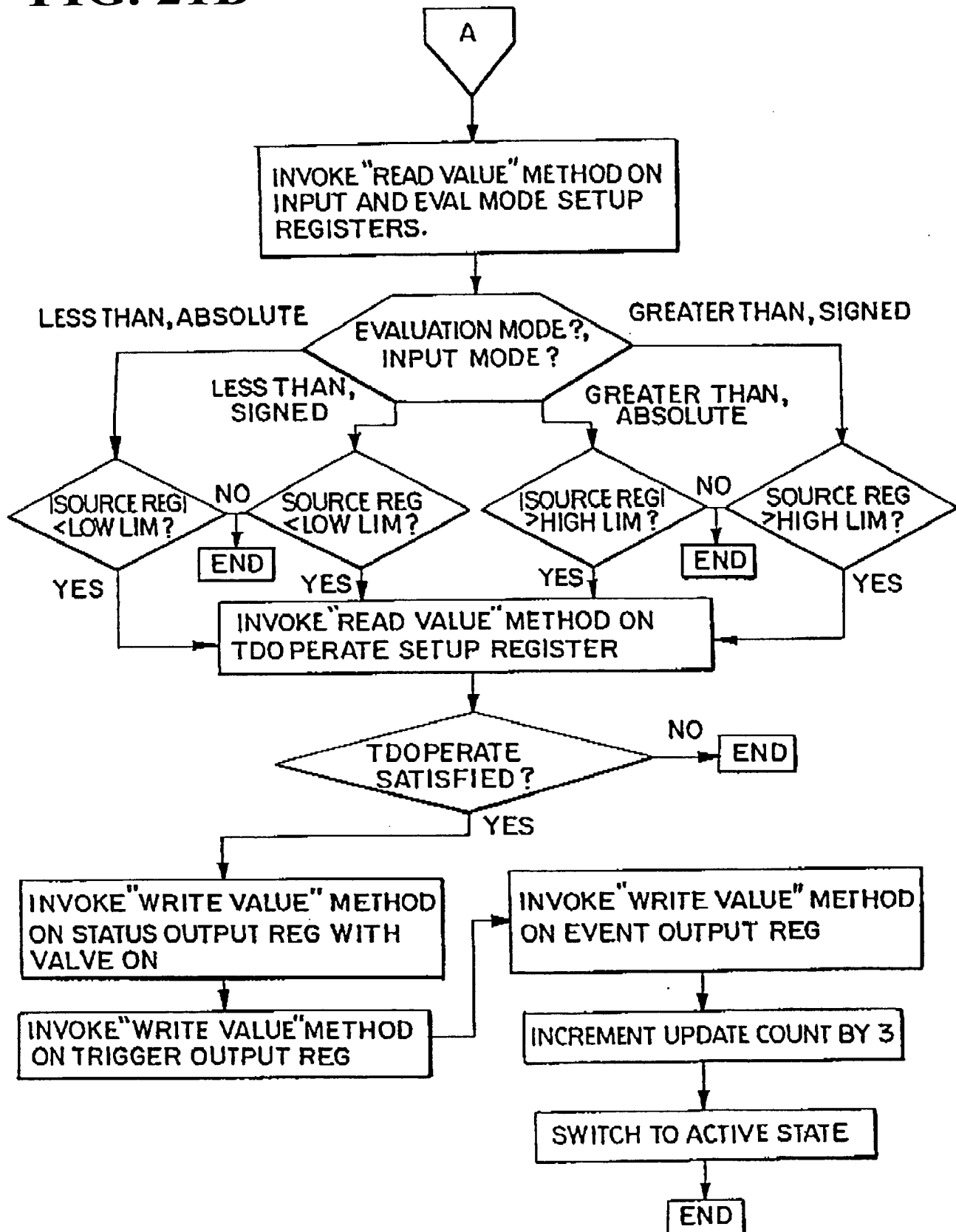


FIG. 21C

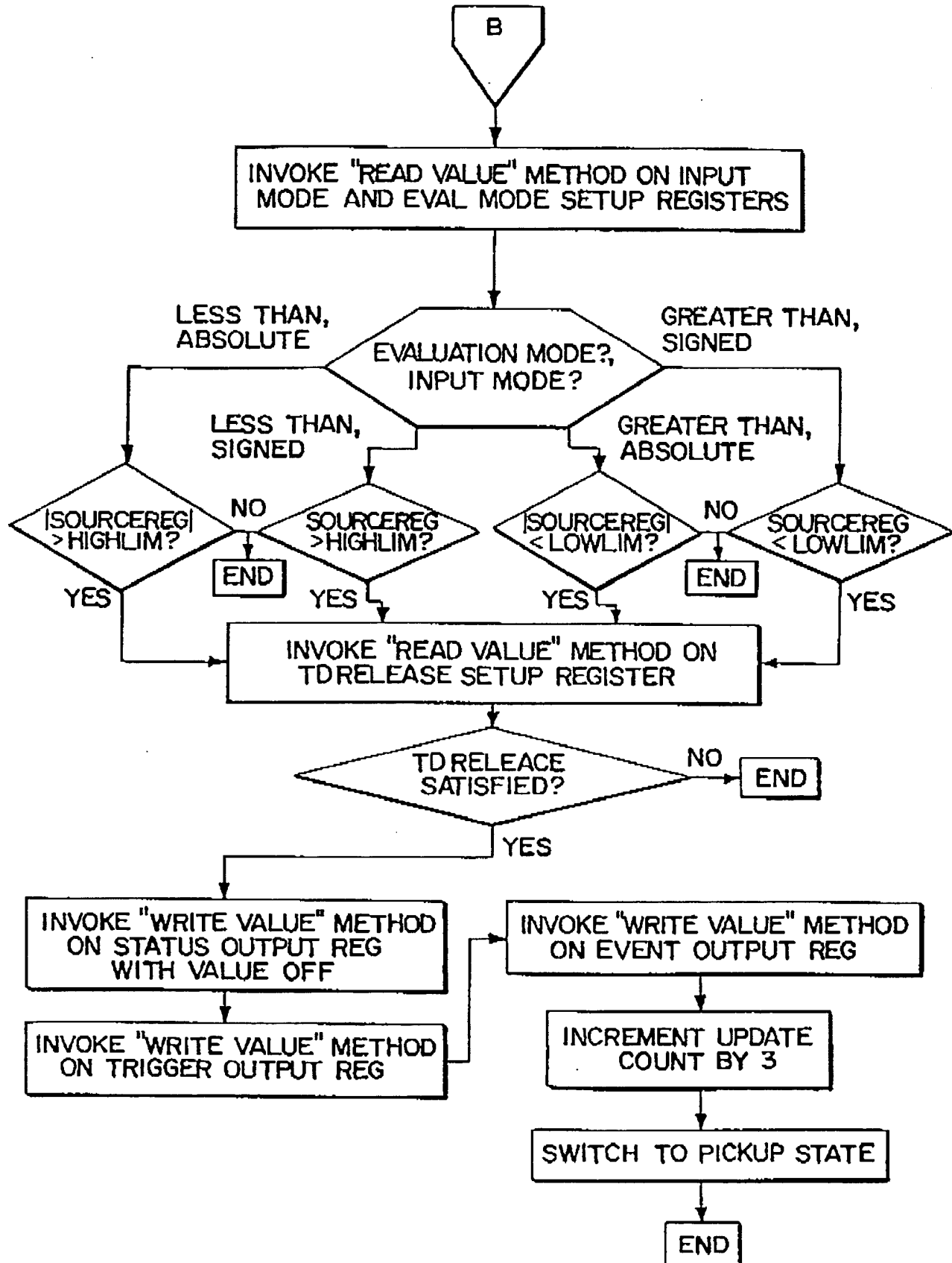


FIG. 22A

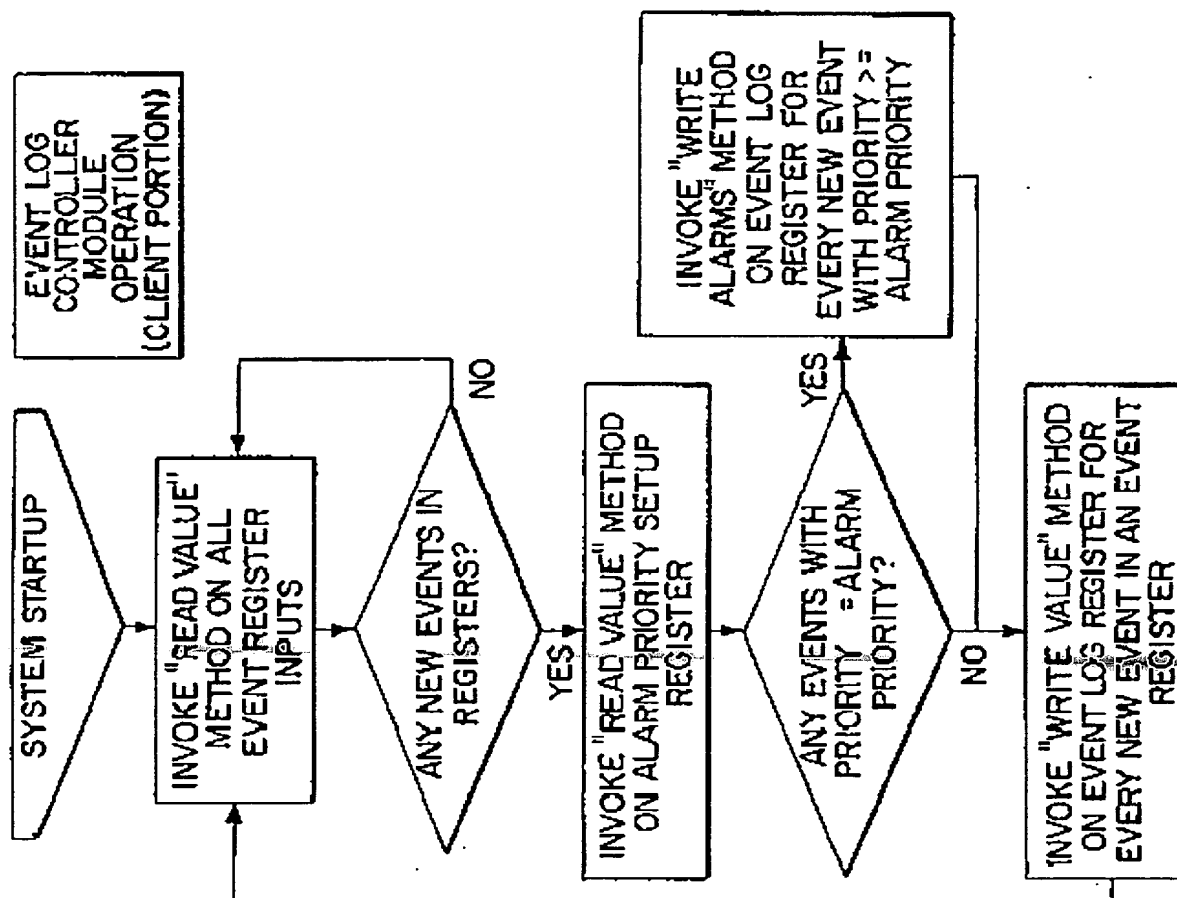


FIG. 22

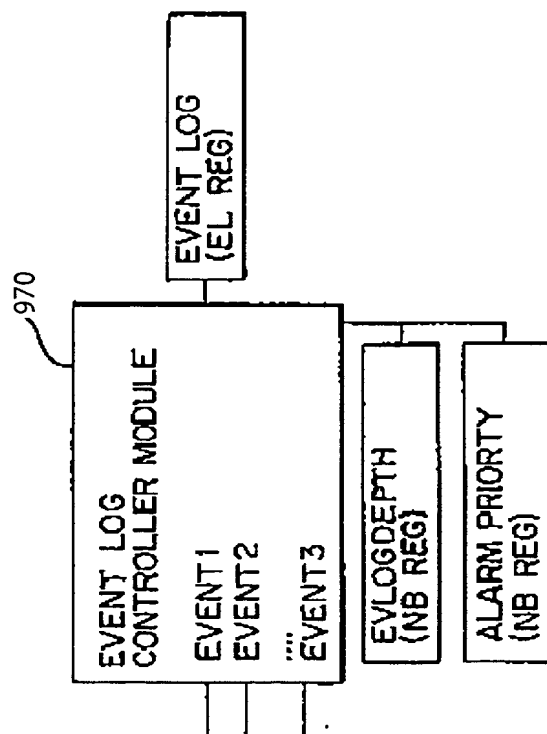


FIG. 23

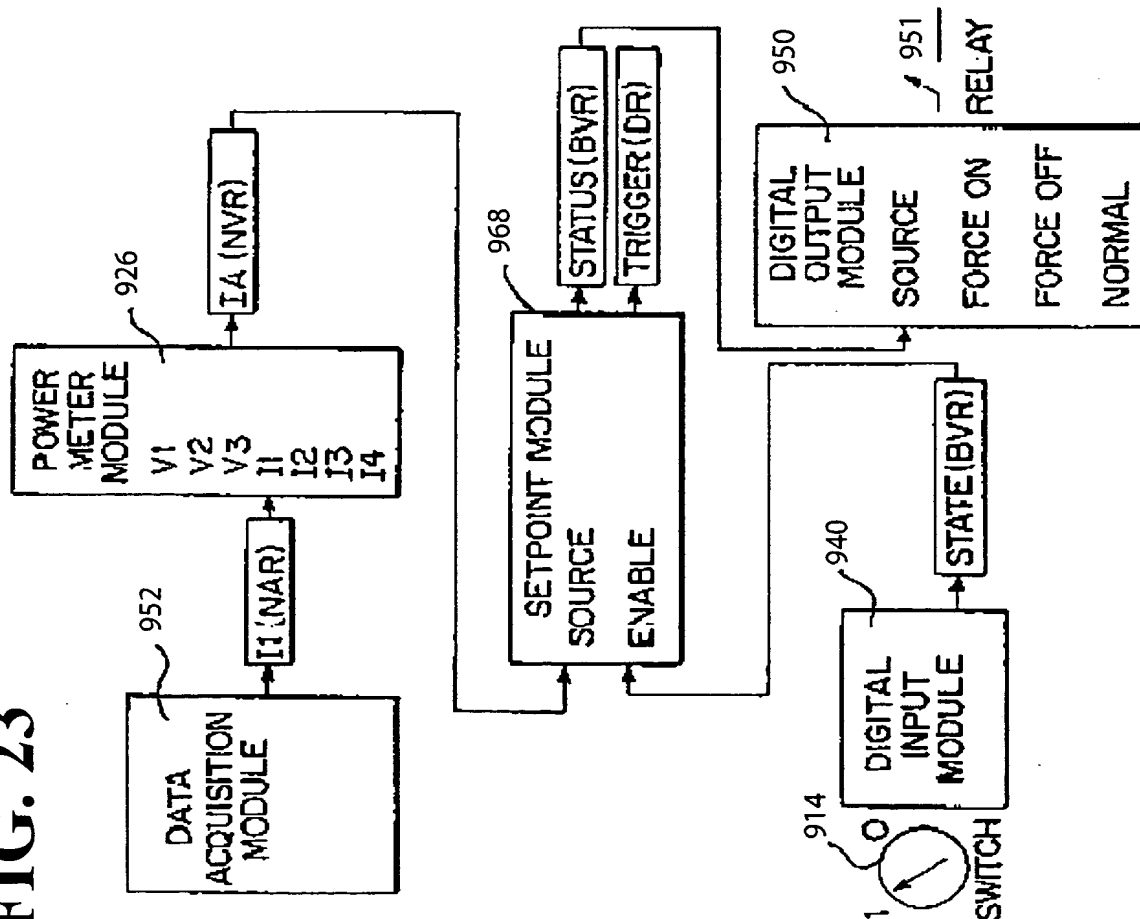


FIG. 24A

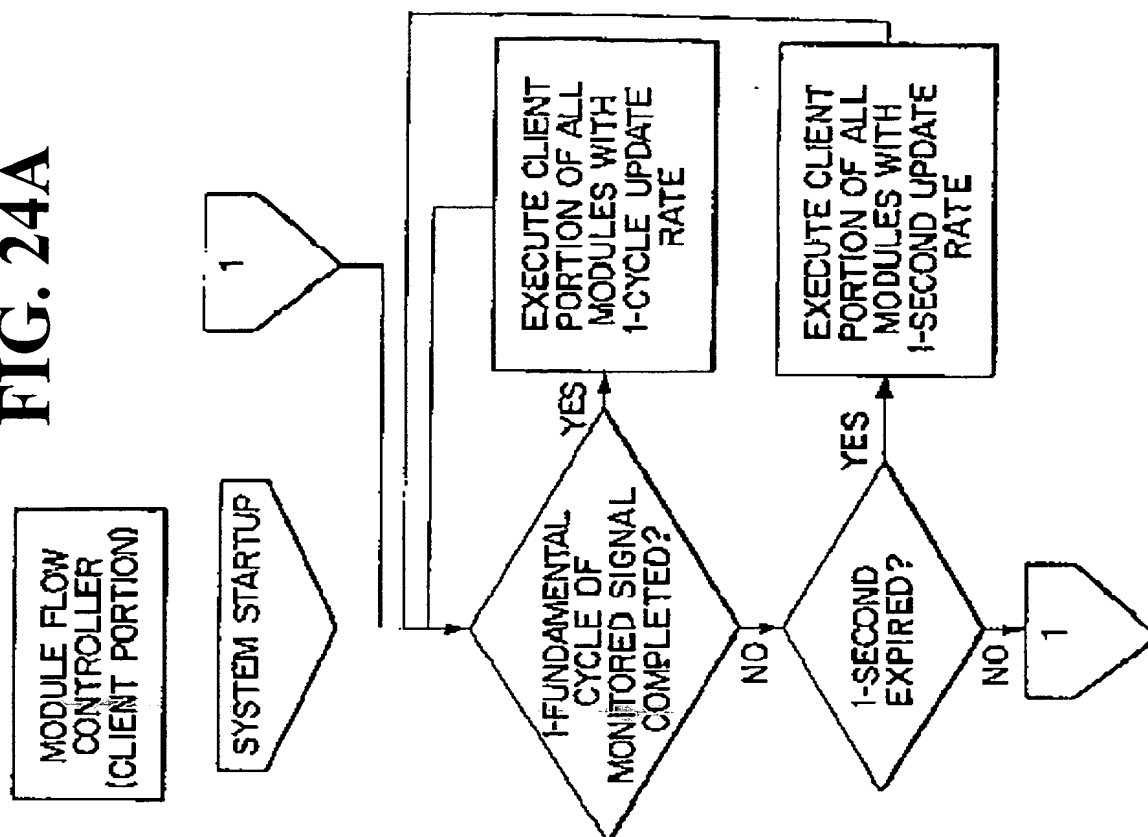


FIG. 25

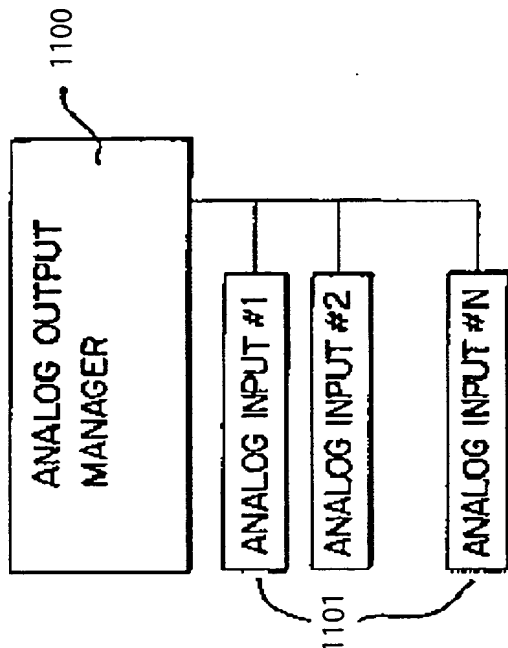


FIG. 24B

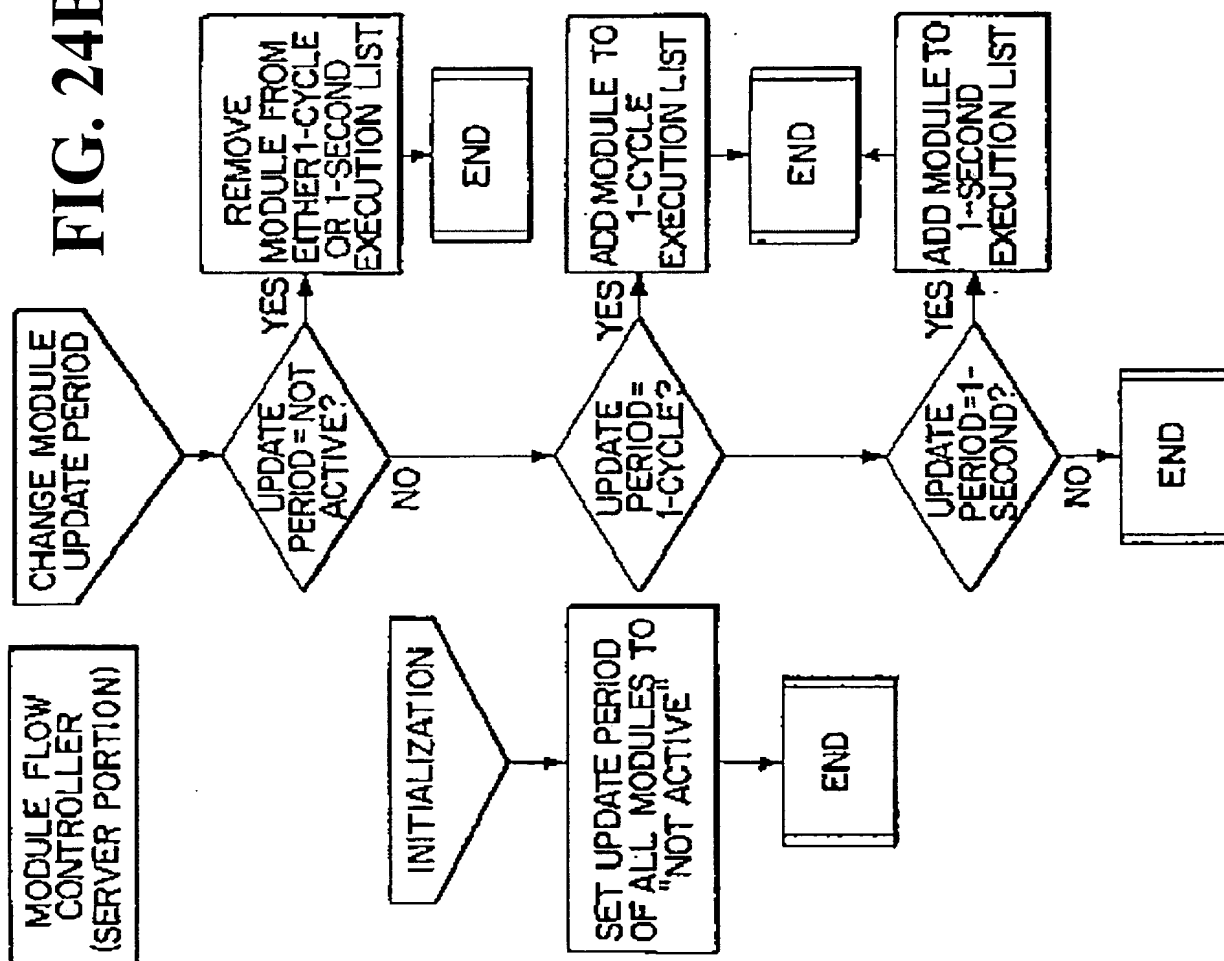


FIG. 25A

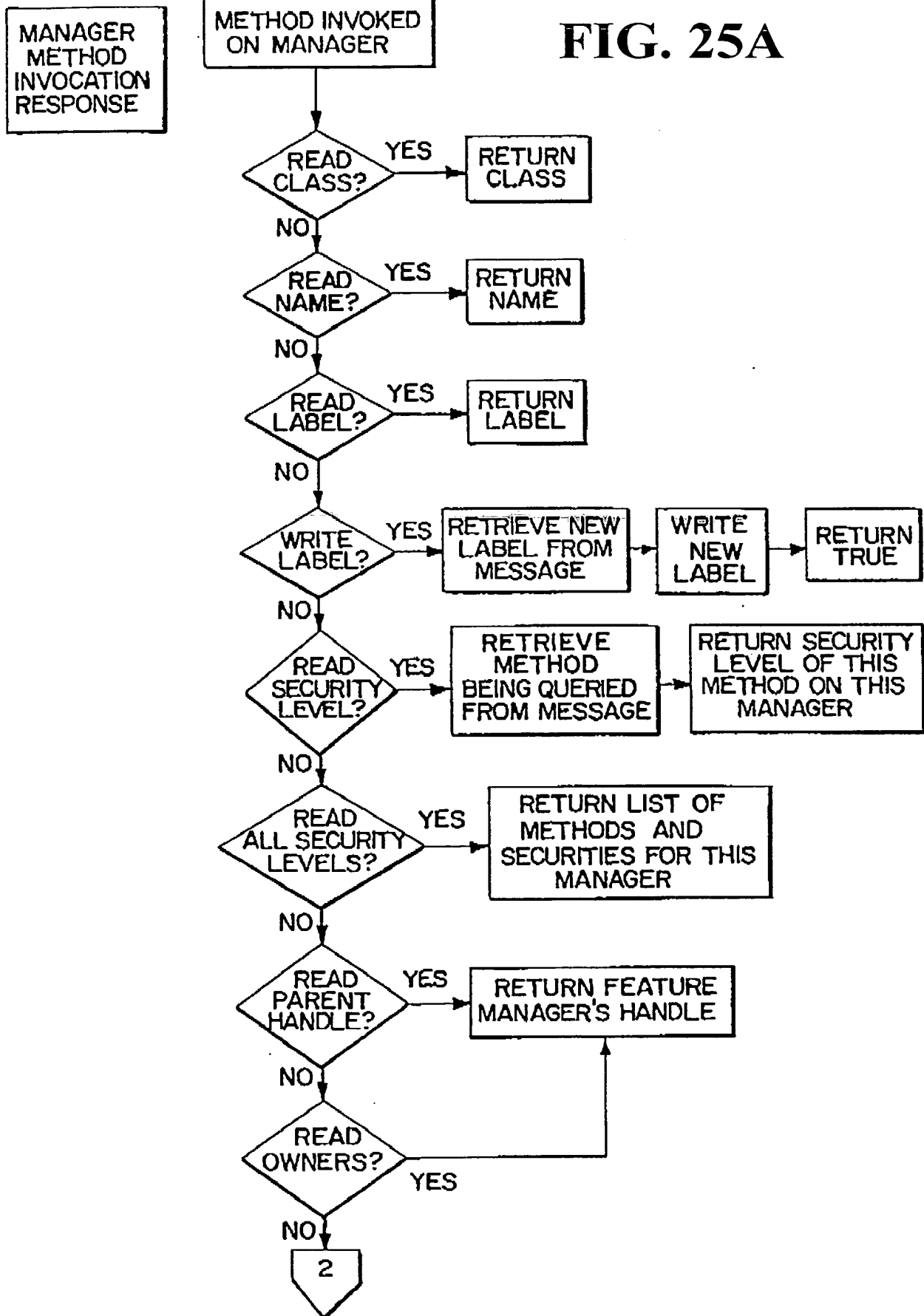


FIG. 25B

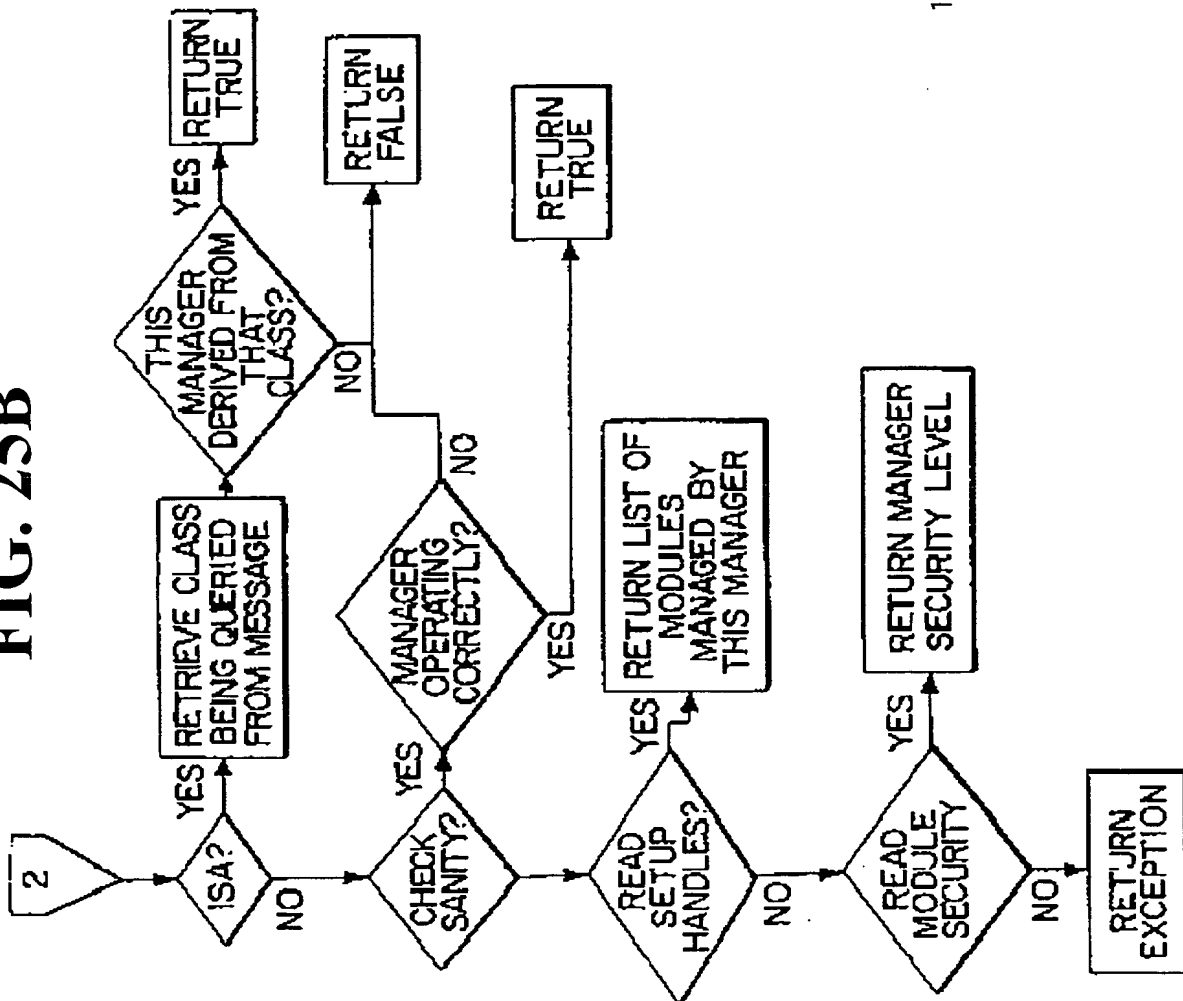
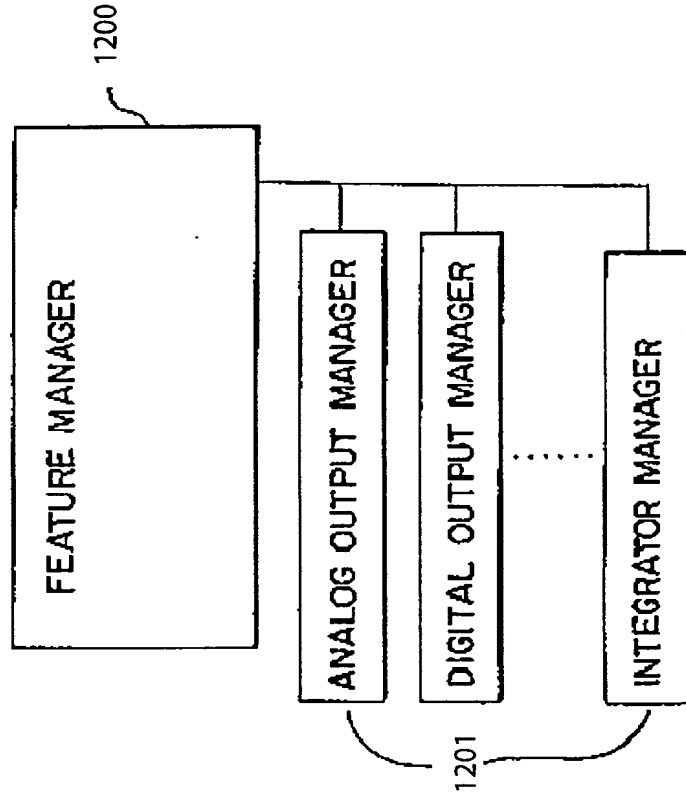


FIG. 26



FEATURE
MANAGER
METHOD
INVOCATION
RESPONSE

FIG. 26A

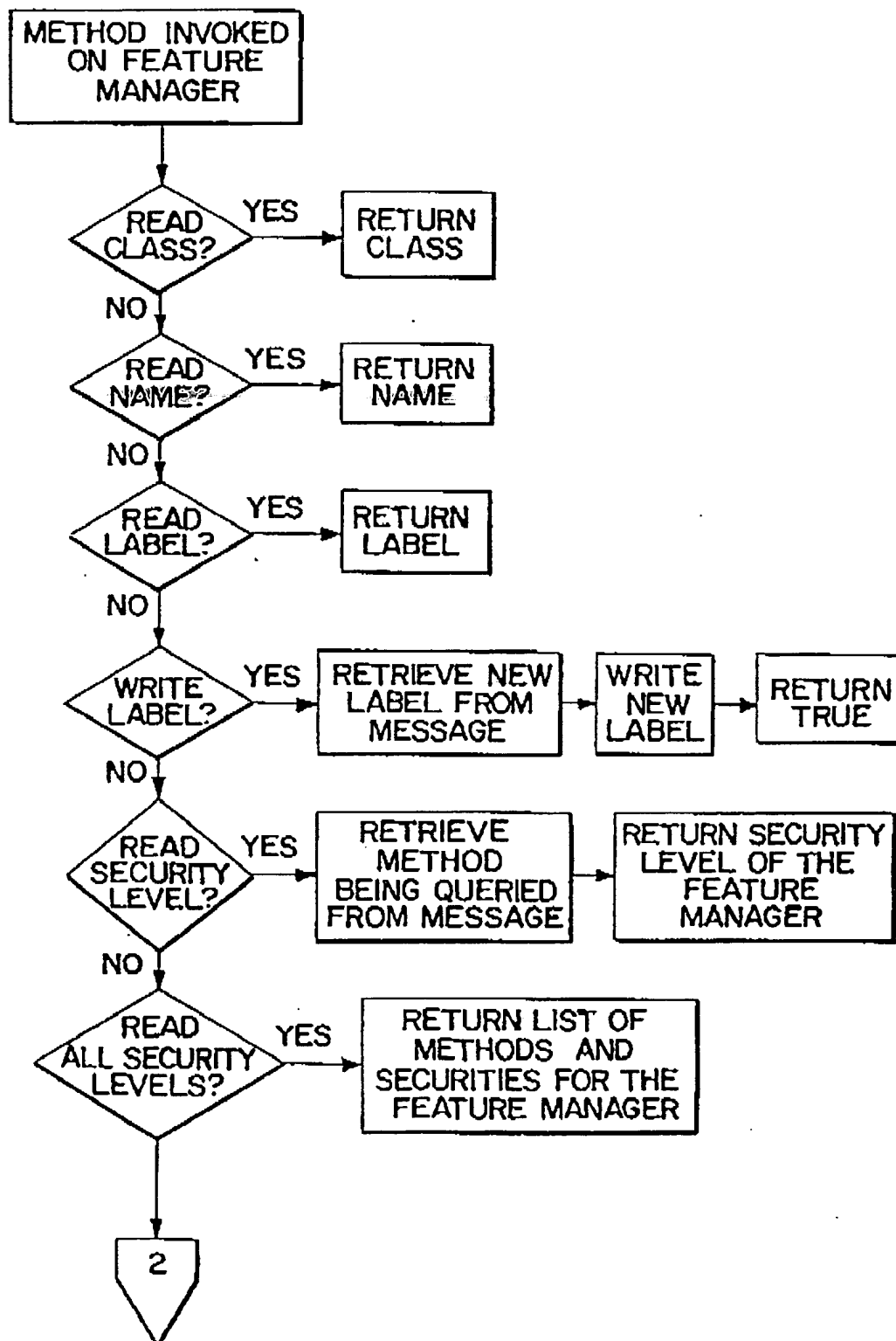
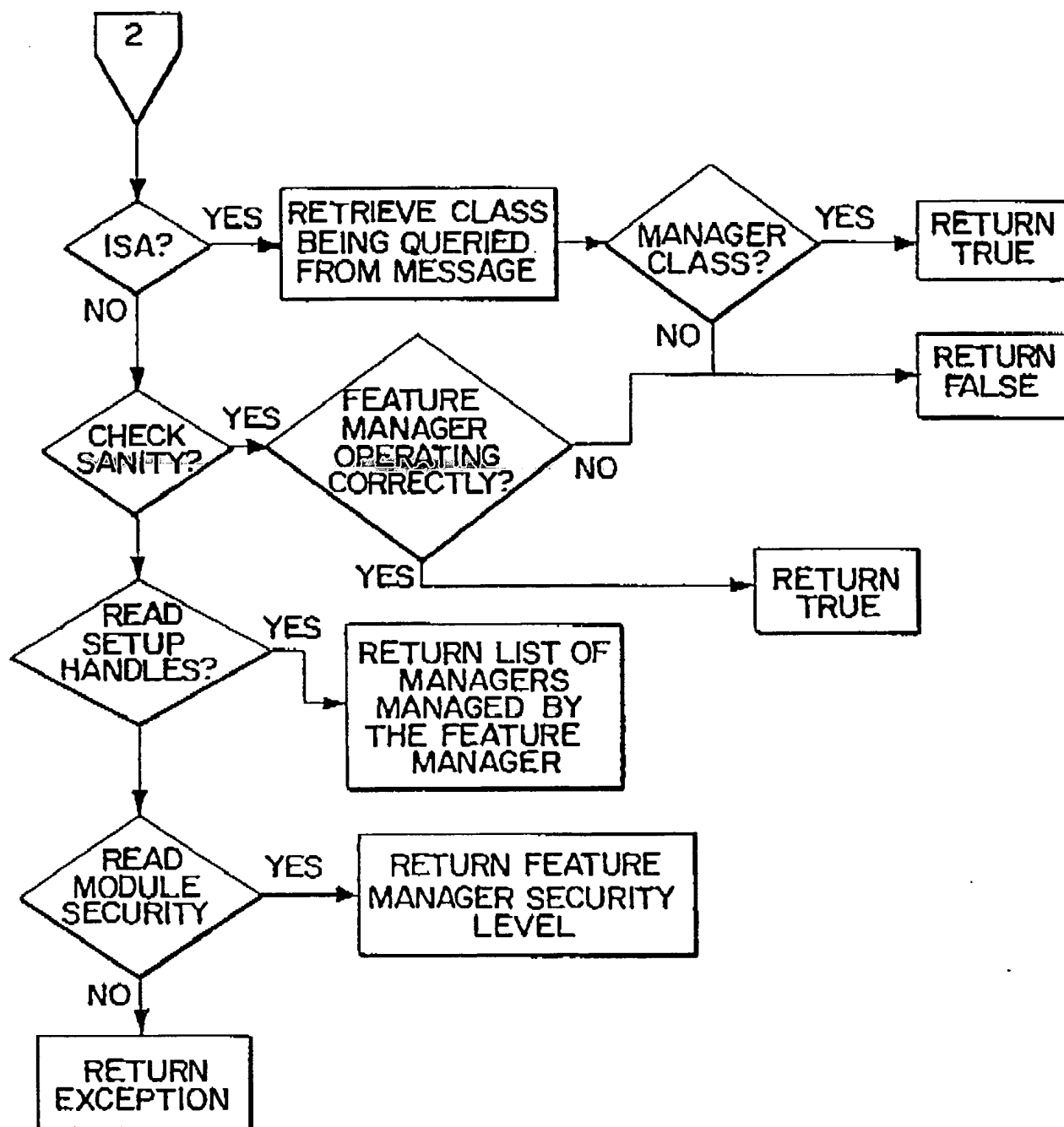


FIG. 26B



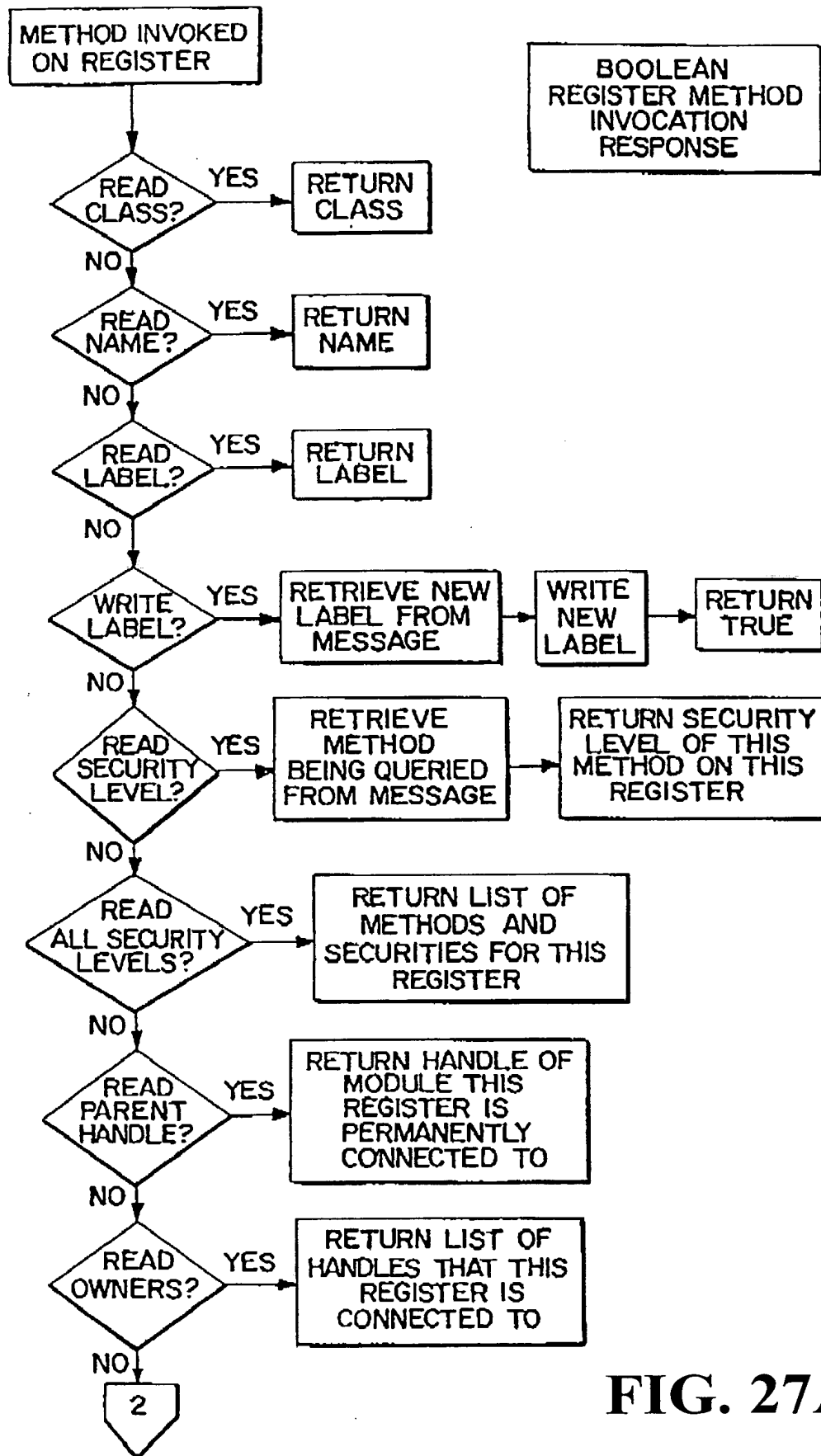


FIG. 27A

FIG. 27B

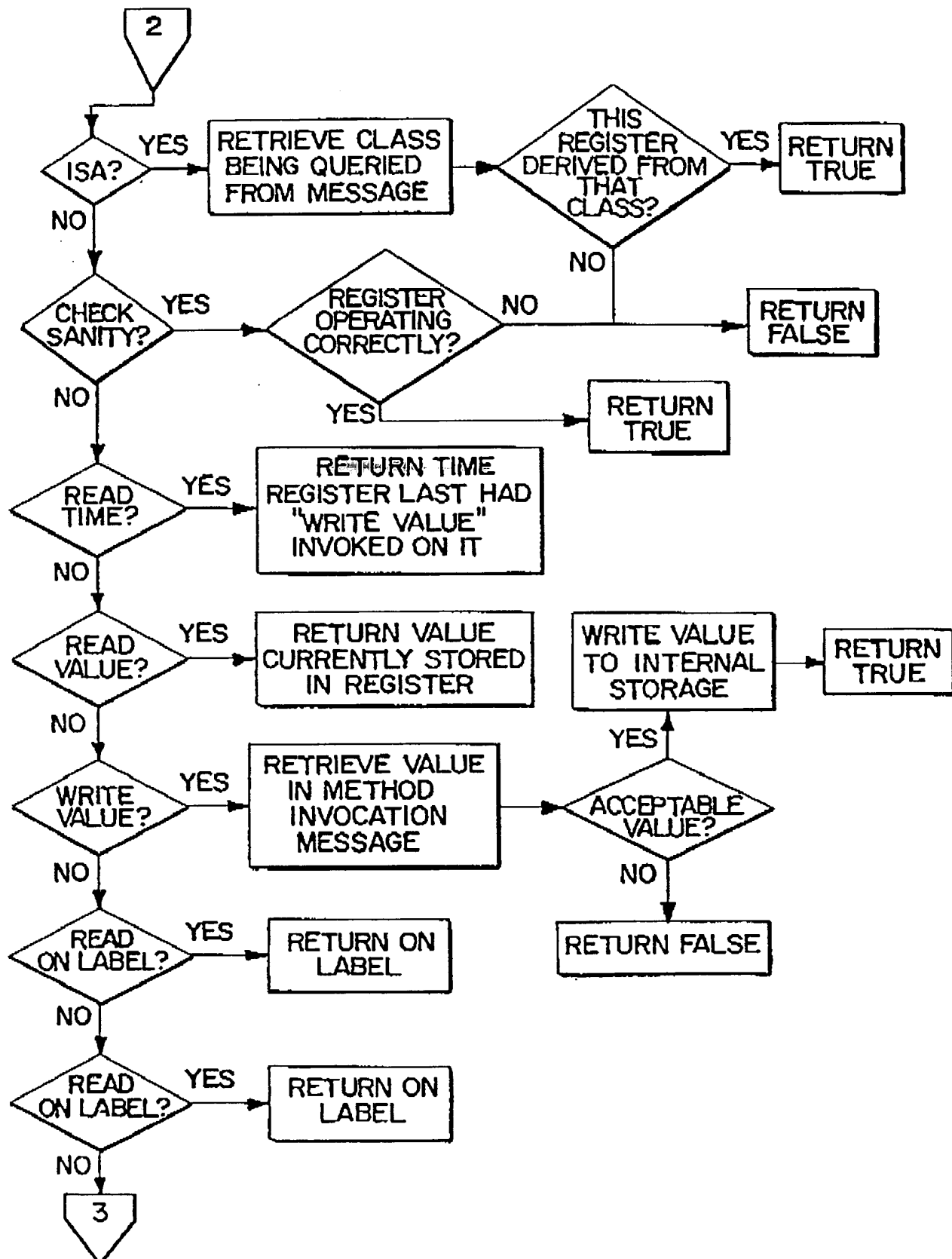


FIG. 27C

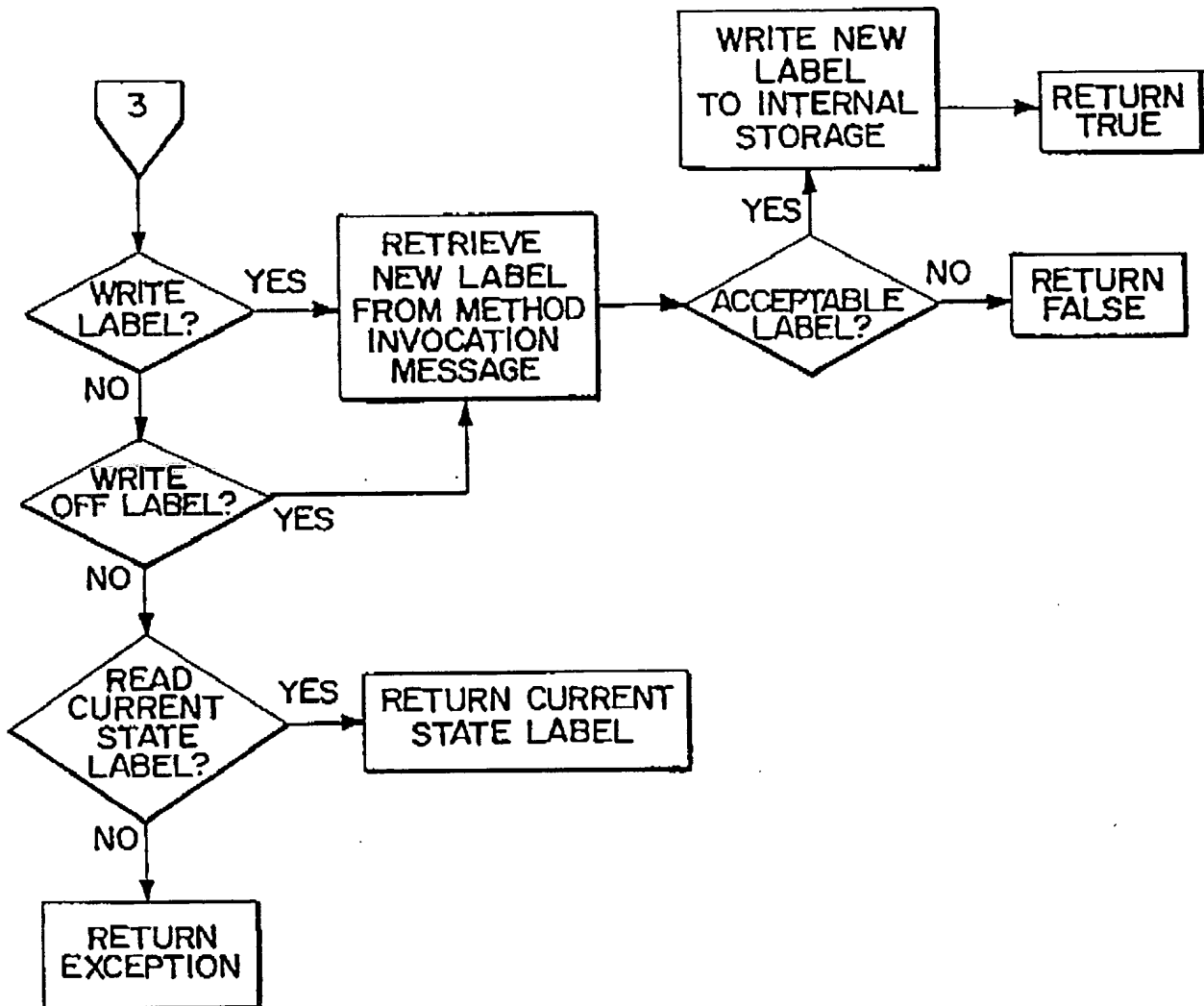


FIG. 28A

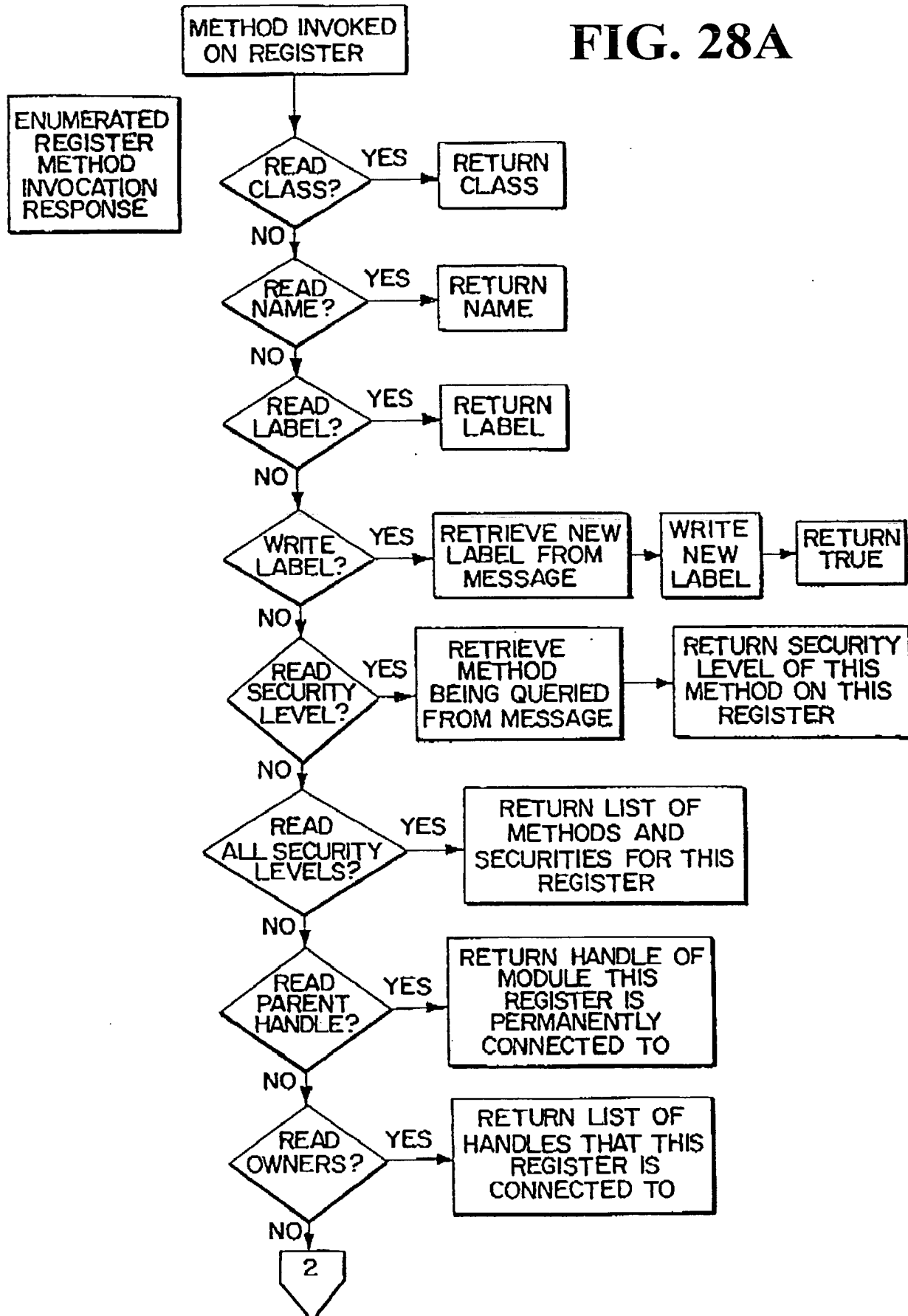


FIG. 28B

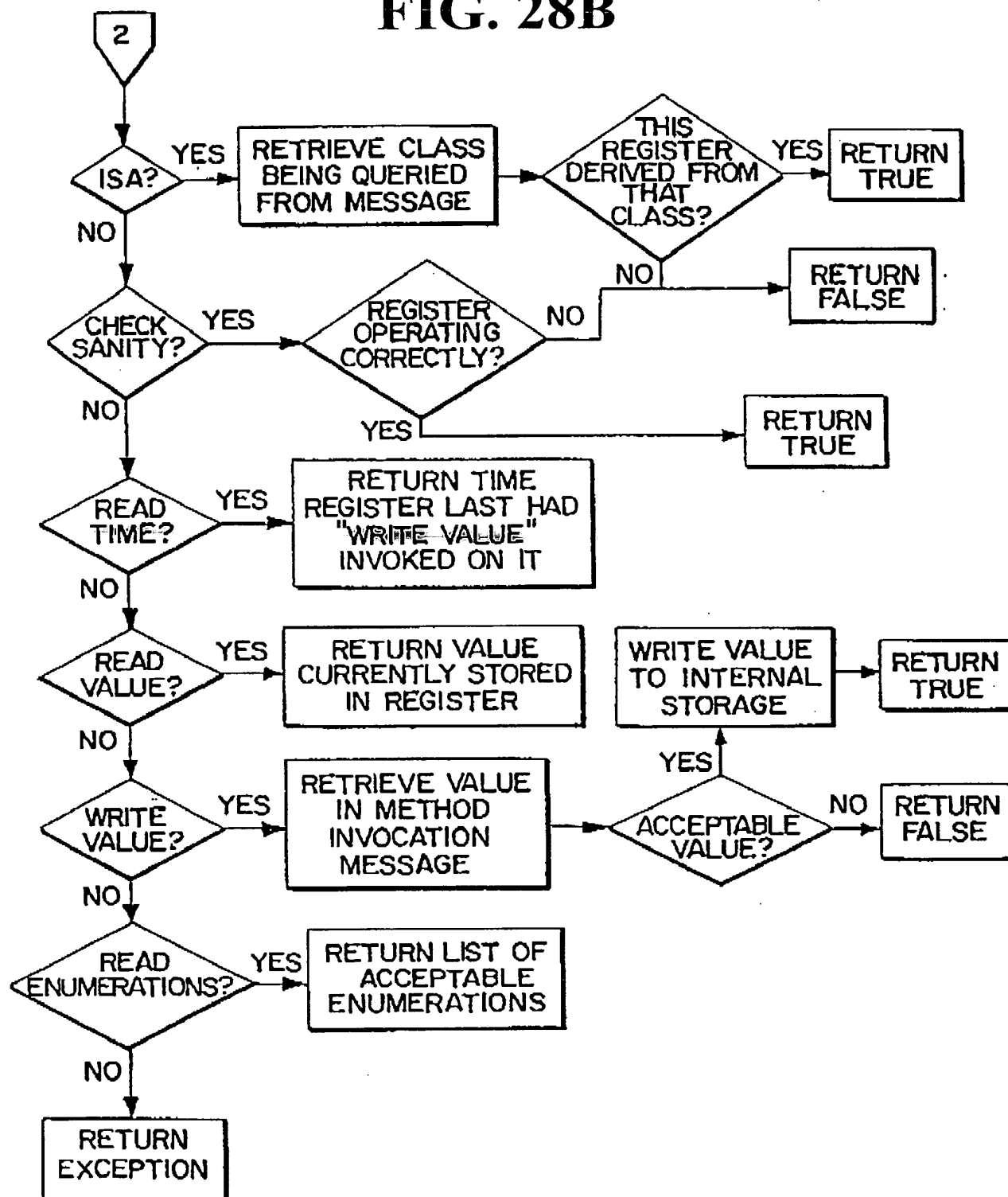


FIG. 29A

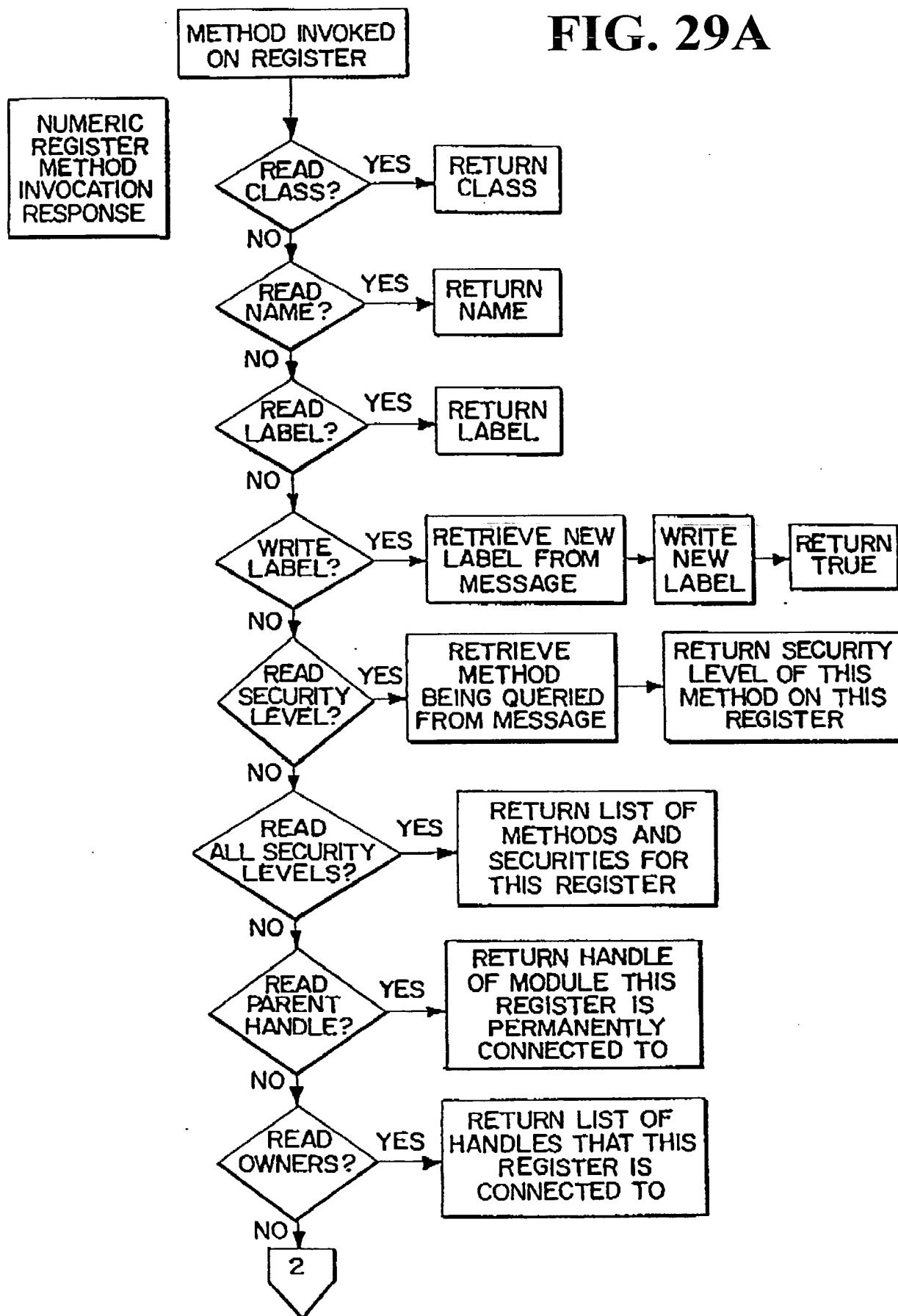


FIG. 29B

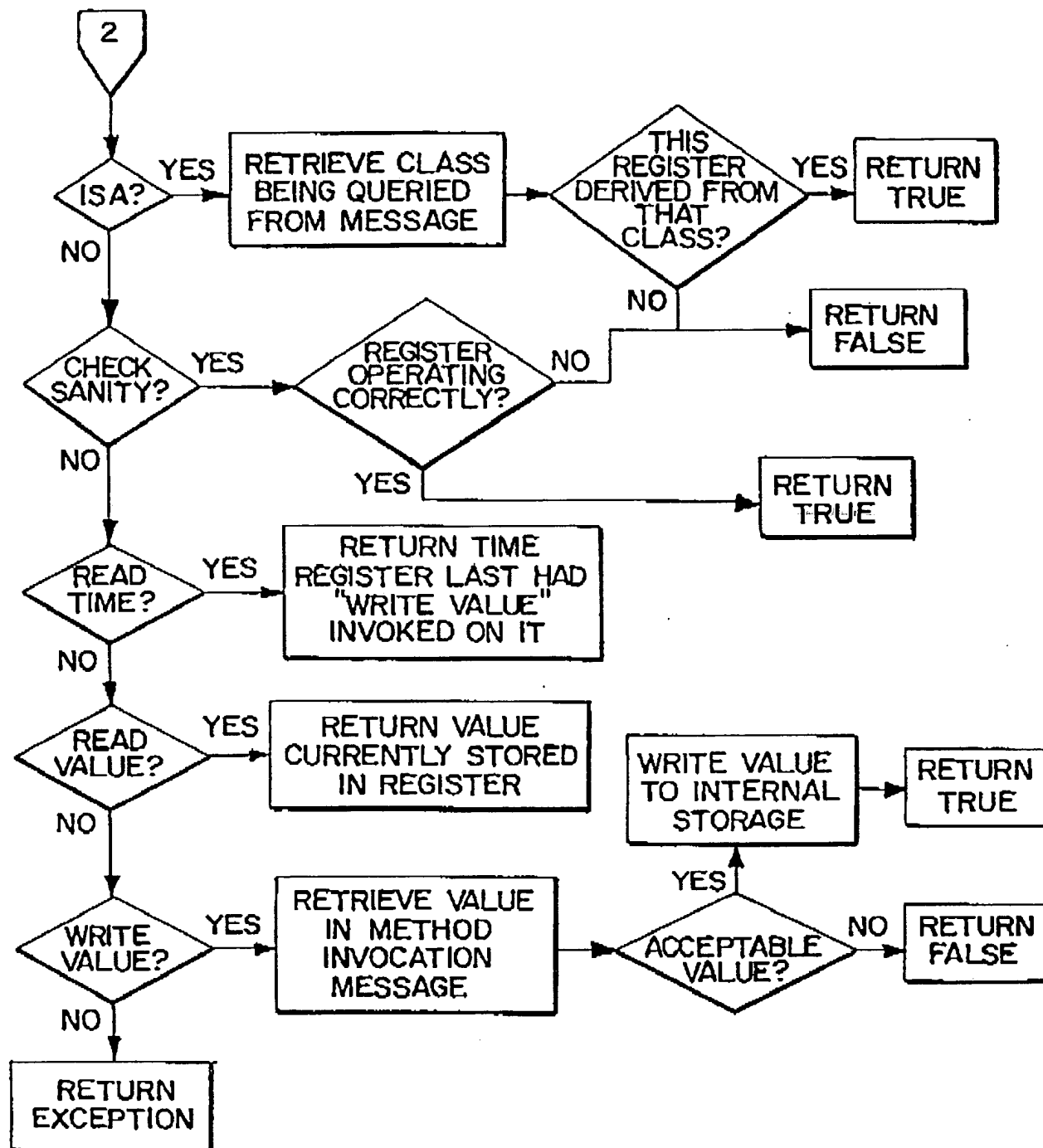


FIG. 30A

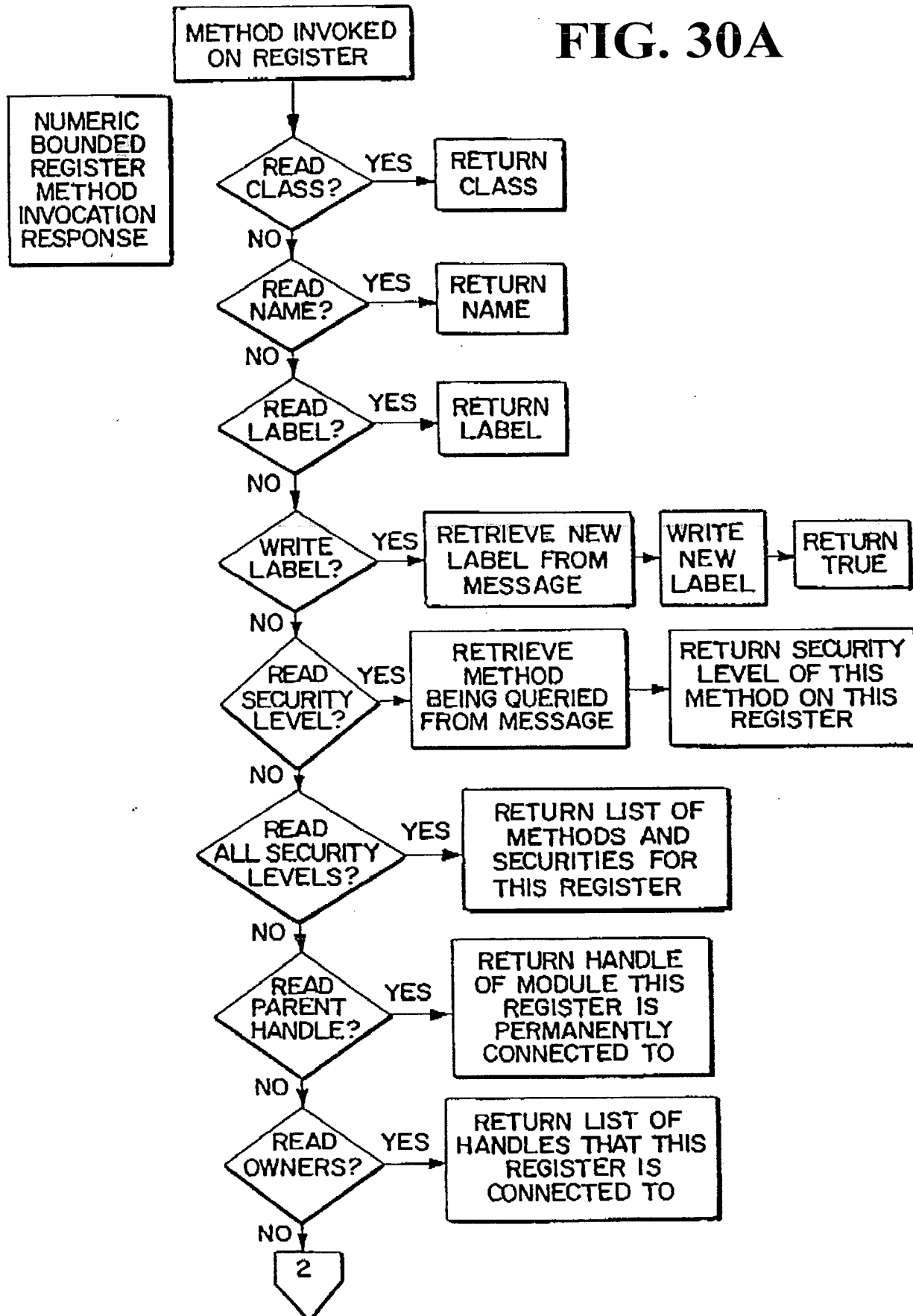


FIG. 30B

